8COM Segment type LCD Driver,5uA typ.

1 Description

The CN90C8S35 is a segment-based LCD driver chip with a duty cycle of 1/8, capable of driving up to 280 segments. It features a low-power design that enables ultra-low power consumption, effectively reducing energy loss.

2 Features

- Fixed 1/4 Bias, 1/8 Duty.
- 35*8 = 280 bits, with built-in buffer amplifier.
- Low power consumption design, 5uA current at typical condition.
- Internal LCD Contrast control Circuit
- No external component required
- Interface: 2 wire serial interfaces
- Compatible with TTL/CMOS
- Integrated reset and oscillator circuits.

3 Key Specifications

- Supply Voltage Range (VDD): 2.5V to 5.5V
- Supply Voltage Range (VLCD): 2.5V to 5.5V
- Operating Temperature Range: -40°C to +125°C
- Frame Rate (fclk): 80Hz (Typ)

4 Applications

- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks
- Home automation

5 Order Information

Product Number	Package	Quantity/Tape
CN90C8S35	TSSOP48	2500/Reel
CN90C8S35L	LQFP48	250/Tray

6 Marking

Product Number	Marking
CN90C8S35	CN90C8S35 YYWWXX LOT No
CN90C8S35L	

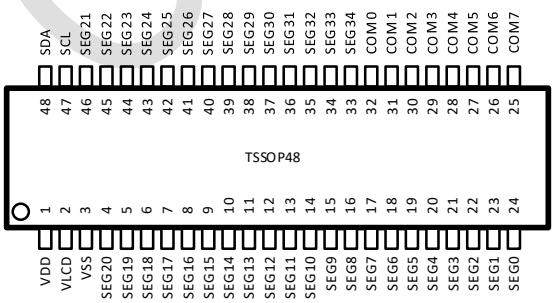
Note: YY=Year WW=Week XX=Factory code

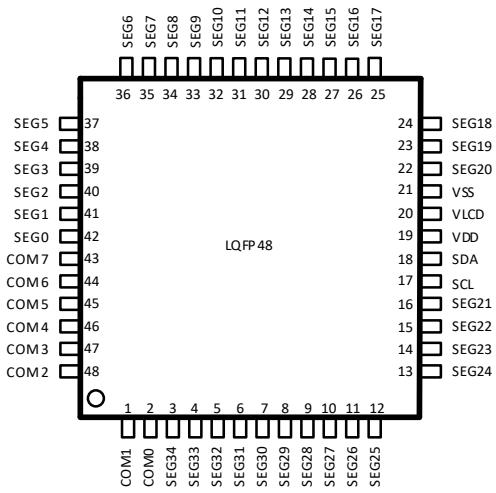
LOT No=Wafer lot number

Green (RoHS & HF): CHIPNORTH defines “Green” to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

7 Pinout

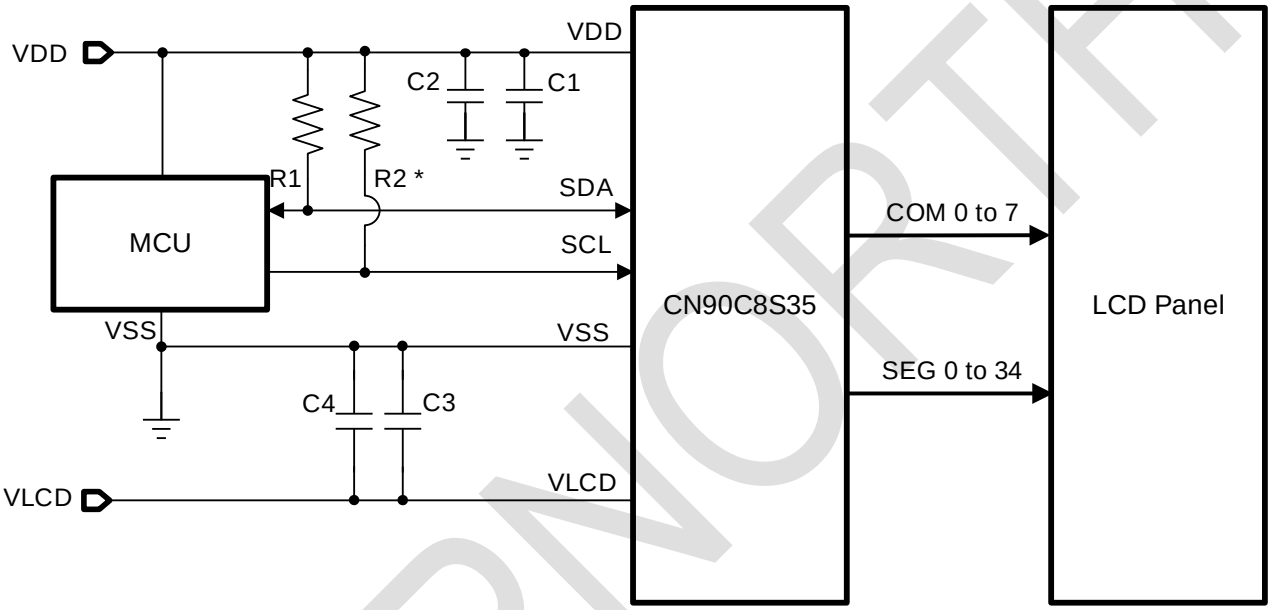




8 Pin Descriptions

Pin Name	I/O	TSSOP48	LQFP48	Function
SDA	I/O	48	18	2-line serial data input and output
SCL	I	47	17	2-line serial clock input
VSS	I	3	21	GND
VDD	I	1	19	Power supply for logic
VLCD	I	2	20	Power supply for LCD drive
SEG0~34	O	24~4,46~33	42~22,16~3	SEGMENT driver output for LCD
COM0~7	O	32~25	2,1,48~43	COMMON driver output for LCD

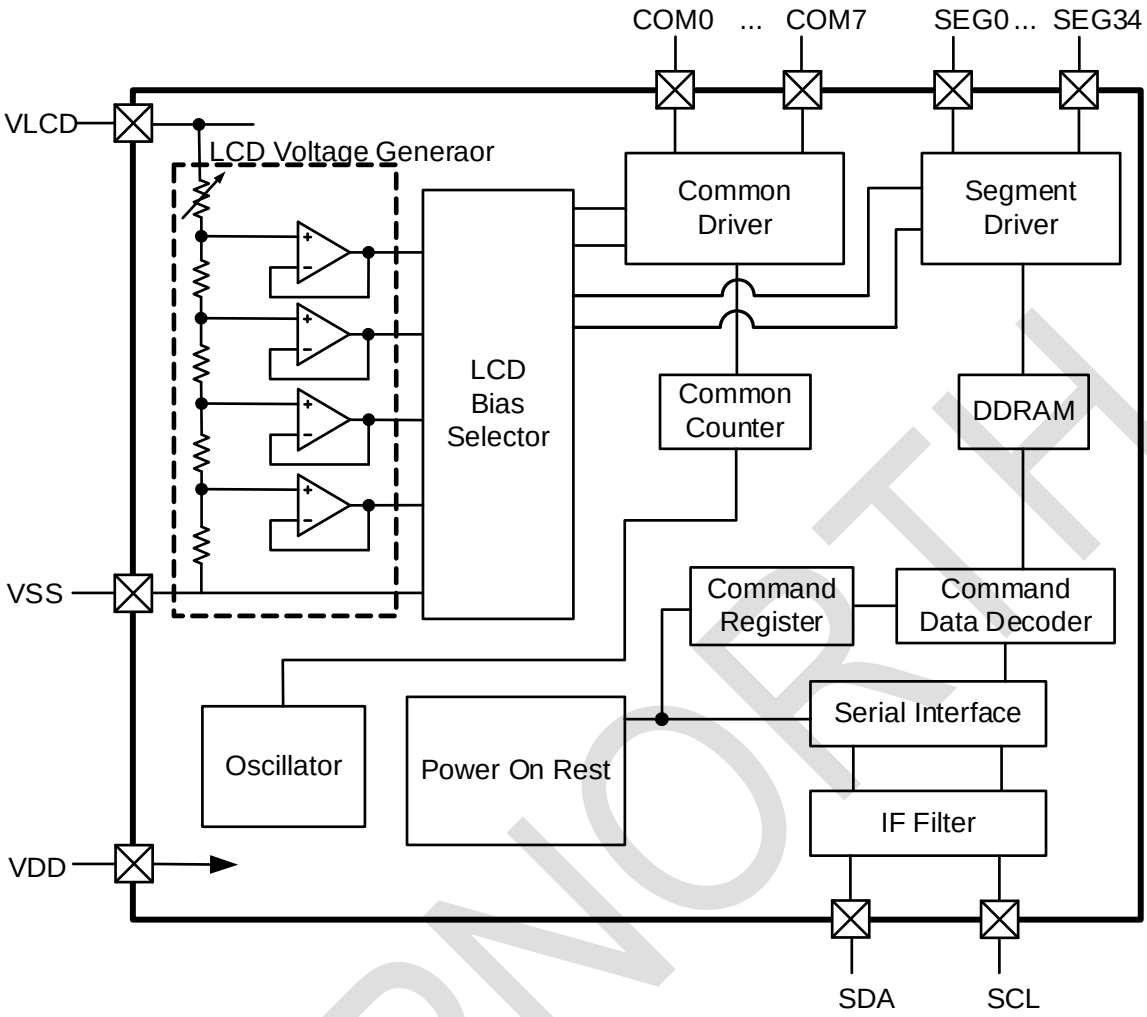
9 Typical Application



Note: 1.* R2 is optional.

2. C1 and C3 are recommended to be 0.1 uF. C2 and C4 are recommended to be 10 uF. The capacitors shall be placed close to the IC pins during layout.

10 Block Diagram



11 Specifications

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3 to +6.5	V	Power supply
Power Supply Voltage 1	V_{LCD}	-0.3 to +6.5	V	LCD drive voltage
Input voltage range	V_{IN}	-0.3 to VDD+0.3	V	
Soldering Temperature	T_{lead}	260（soldering，10s）	°C	
Operational temperature range	T_{opr}	-40 to +125	°C	
Storage temperature range	T_{stg}	-55 to +150	°C	

Note: Operating beyond the absolute maximum rated values may result in IC damage.

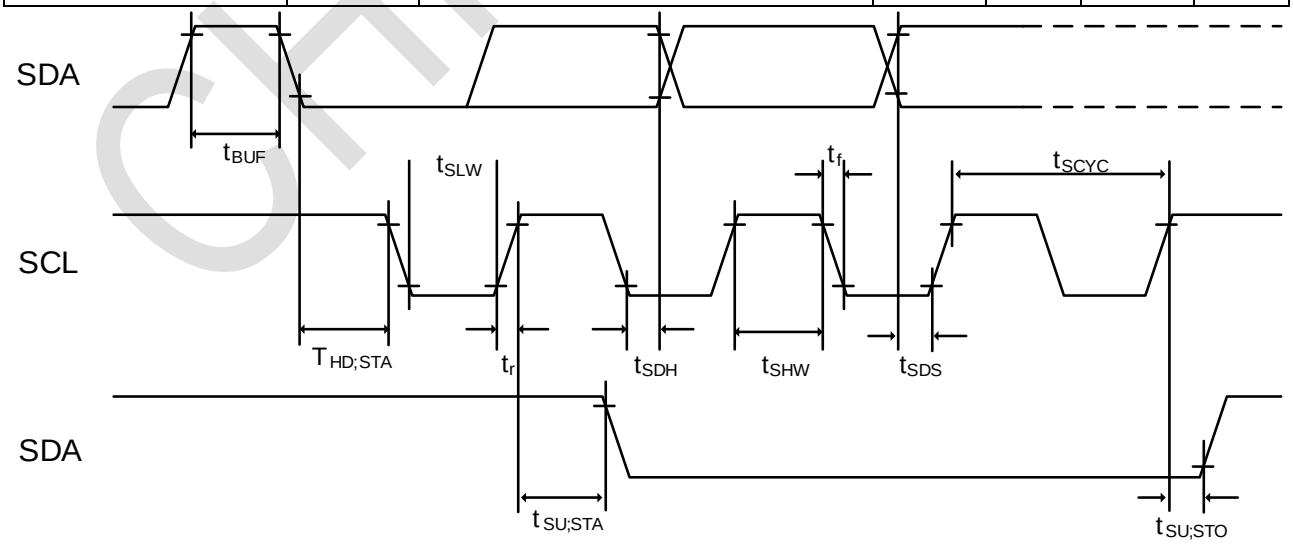
11.2 Recommended Operating Ratings(Ta=-40°C to +125°C,VSS=0V)

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Power Supply Voltage1	V_{DD}	2.5	-	5.5	V	Power supply
Power Supply Voltage2	V_{LCD}	2.5	-	5.5	V	LCD drive voltage

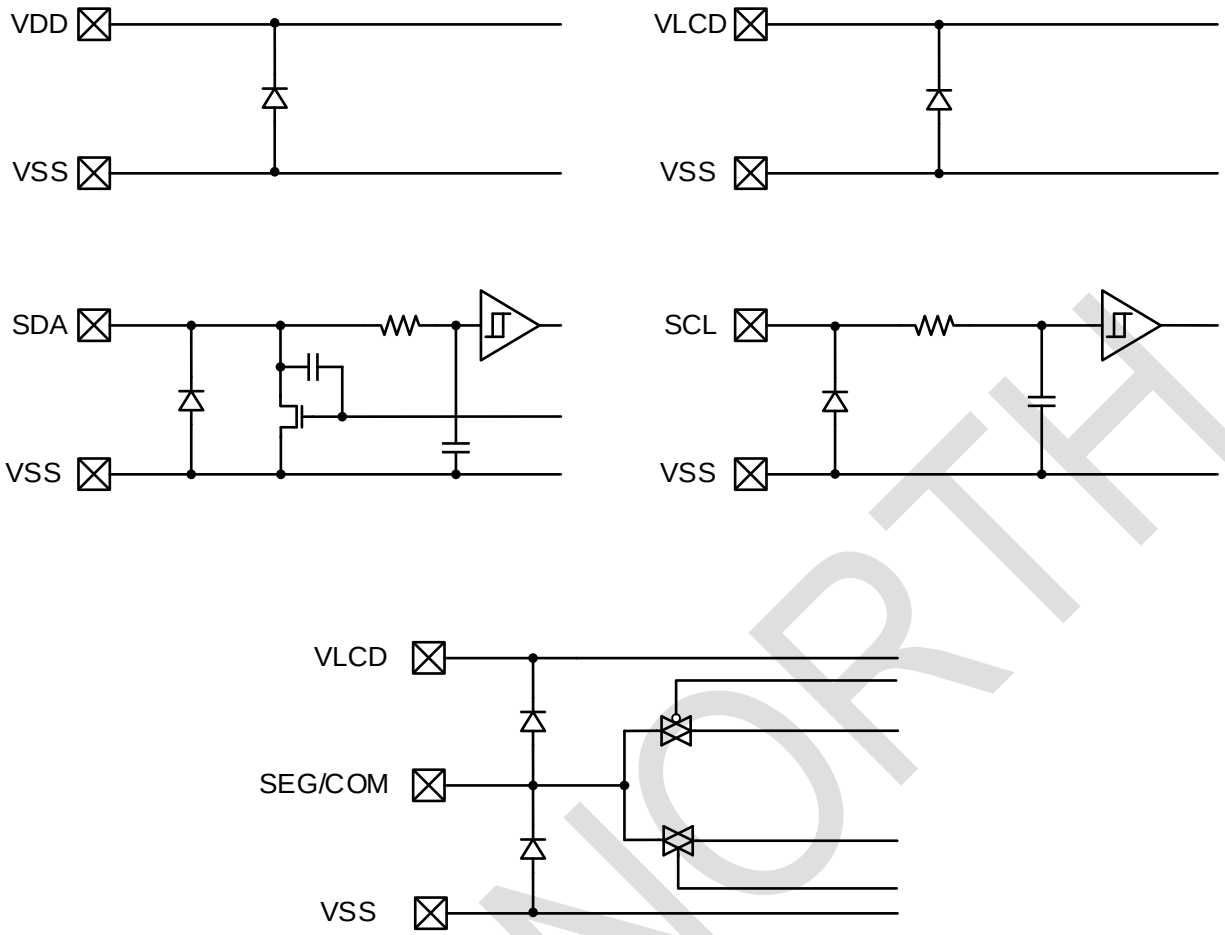
11.3 Electrical Characteristics

DC Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +125°C, unless otherwise specified)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
"H" level input voltage		V_{IH}	SDA,SCL	1.4	-	VDD	V
"L" level input voltage		V_{IL}	SDA,SCL	VSS	-	0.4	V
"H" level input current		I_{IH}	SDA,SCL	-	-	1	μA
"L" level input current		I_{IL}	SDA,SCL	-1	-	-	μA
LCD driver on resistance	SEG	R_{ON}	Iload=±10μA	-	3.5	-	kΩ
	COM	R_{ON}		-	3.5	-	kΩ
Standby current		I_{ST}	Display off, Oscillation off	-	-	1	μA
Power consumption 1		I_{DD}	VDD=3.3V,VLCD=5V,Ta=25°C, Power save mode1, FR=80Hz,1/4 bias, Frame inversion	-	2.5	5	μA
Power consumption 2		I_{LCD}	VDD=3.3V,VLCD=5V,Ta=25°C, Power save mode1, FR=80Hz,1/4 bias, Frame inversion	-	4.7	10	μA
Frame frequency		f_{CLK}	FR = 80Hz, VDD=3.3V	-	80	-	Hz
Input rise time		t_r	-	-	-	0.3	μs
Input fall time		t_f	-	-	-	0.3	μs
SCL cycle time		t_{SCYC}	-	2.5	-	-	μs
SCL "H" pulse		t_{SHW}	-	0.6	-	-	μs
SCL "L" pulse		t_{SLW}	-	1.2	-	-	μs
SDA setup time		t_{SDS}	-	700	-	-	ns
SDA hold time		t_{SDH}	-	0	-	-	ns
IIC free time		t_{BUF}	-	1.3	-	-	μs
START hold time		$t_{HD;STA}$	-	0.6	-	-	μs
START setup time		$t_{SU;STA}$	-	0.6	-	-	μs
STOP setup time		$t_{SU;STO}$	-	0.6	-	-	μs

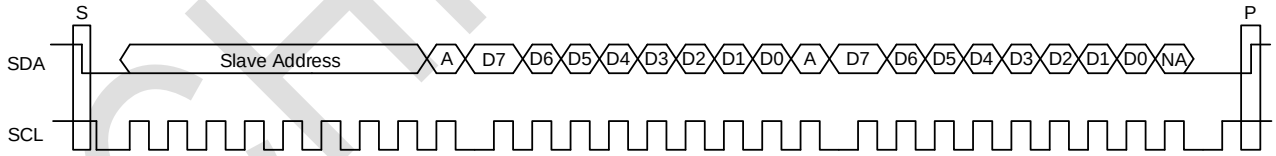


12 I/O equivalent circuit



13 Command Registers Description

D7 It is the judgment of command or data bit;
C=0,Represents the next byte（D7~D0）is write data
C=1,Represents the next byte is command



	D7	D6	D5	D4	D3	D2	D1	D0
ADSET	**C**	**0**	P[5:0]					
EVRSET	**C**	**1**	**0**	EVR[4:0]				
DISCTL	**C**	**1**	**1**	**0**	FR[1:0]		SR[1:0]	
ICSET	**C**	**1**	**1**	**1**	**0**	LF	RST	EN
APCTL	**C**	**1**	**1**	**1**	**1**	**0**	AON	AOFF

Name	Default	Description
P[5:0]	000000	DDRAM address. The address range can be set from 00 to 22 (Hex). Addresses outside this range are not permitted; if set, the address will default to “000000”.
FR[1:0]	00	To save power, set the frame frequency as follows: 00: 80Hz, Normal Mode 01: 70Hz, Power Mode 1 10: 64Hz, Power Mode 2 11: 50Hz, Power Mode 3 *The current consumption decreases in the following order: Normal Mode > Power Mode 1 > Power Mode 2 > Power Mode 3.
SR[1:0]	10	To conserve power, set the internal bias current as follows: 00: ×0.5, Power Save Mode 1 01: ×0.67, Power Save Mode 2 10: ×1.0, Normal Mode 11: ×1.8, High Power Mode *The current consumption increases in the following order: Power Save Mode 1 < Power Save Mode 2 < Normal Mode < High Power Mode.
LF	1	Set Line or Frame Inversion Mode: 0: Line Inversion 1: Frame Inversion Operation current: Line inversion > Frame inversion For drive mode of Line inversion and Frame inversion, refer to LCD waveform.
RST	0	Setting '1' will reset all command registers in this table, but will not reset the display data in DDRAM. Note: Do not set LF and EN simultaneously during the reset.
EN	0	0: Display Off 1: Display On Display Off: This command does not affect the data in DDRAM. All COM and SEG outputs stop after one frame. The “Display Off” mode ends when “Display On” is set. Display On: COM and SEG outputs are activated, allowing data from DDRAM to be read and displayed.
AON AOFF	00	Control Pixel Display: 00: Normal Mode 01: All Pixels OFF. Turns off all pixels (independent of DDRAM data). 10: All Pixels ON. Lights up all pixels (independent of DDRAM data). 11: Same as 01. Turns off all pixels (independent of DDRAM data). The AON/AOFF commands are only effective when the display is on (EN=1) and do not alter DDRAM data.
EVR[4:0]	00000	Display Contrast Setting: For detailed information, refer to the table relating the highest voltage V0 to VLCD.

14 Maximum voltage V0 and VLCD relationship table

EVR	Calculation formula	VLCD =5.500	VLCD =5.000	VLCD =4.000	VLCD =3.500	VLCD =3.000	VLCD =2.500	Unit
0	VLCD	V0=5.500	V0=5.000	V0=4.000	V0=3.500	V0=3.000	V0=2.500	[V]
1	0.967*VLCD	V0=5.323	V0=4.839	V0=3.871	V0=3.387	V0=2.903	V0=2.419	[V]
2	0.937*VLCD	V0=5.156	V0=4.688	V0=3.750	V0=3.281	V0=2.813	V0=2.344	[V]
3	0.909*VLCD	V0=5.000	V0=4.545	V0=3.636	V0=3.182	V0=2.727	V0=2.273	[V]
4	0.882*VLCD	V0=4.853	V0=4.412	V0=3.529	V0=3.088	V0=2.647	V0=2.206	[V]
5	0.857*VLCD	V0=4.714	V0=4.286	V0=3.429	V0=3.000	V0=2.571	V0=2.143	[V]
6	0.833*VLCD	V0=4.583	V0=4.167	V0=3.333	V0=2.917	V0=2.500	V0=2.083	[V]
7	0.810*VLCD	V0=4.459	V0=4.054	V0=3.243	V0=2.838	V0=2.432	V0=2.027	[V]
8	0.789*VLCD	V0=4.342	V0=3.947	V0=3.158	V0=2.763	V0=2.368	V0=1.974	[V]
9	0.769*VLCD	V0=4.231	V0=3.846	V0=3.077	V0=2.692	V0=2.308	V0=1.923	[V]
10	0.750*VLCD	V0=4.125	V0=3.750	V0=3.000	V0=2.625	V0=2.250	V0=1.875	[V]
11	0.731*VLCD	V0=4.024	V0=3.659	V0=2.927	V0=2.561	V0=2.195	V0=1.829	[V]
12	0.714*VLCD	V0=3.929	V0=3.571	V0=2.857	V0=2.500	V0=2.143	V0=1.786	[V]
13	0.697*VLCD	V0=3.837	V0=3.488	V0=2.791	V0=2.442	V0=2.093	V0=1.744	[V]
14	0.681*VLCD	V0=3.750	V0=3.409	V0=2.727	V0=2.386	V0=2.045	V0=1.705	[V]
15	0.666*VLCD	V0=3.667	V0=3.333	V0=2.667	V0=2.333	V0=2.000	V0=1.667	[V]
16	0.652*VLCD	V0=3.587	V0=3.261	V0=2.609	V0=2.283	V0=1.957	V0=1.630	[V]
17	0.638*VLCD	V0=3.511	V0=3.191	V0=2.553	V0=2.234	V0=1.915	V0=1.596	[V]
18	0.625*VLCD	V0=3.438	V0=3.125	V0=2.500	V0=2.188	V0=1.875	V0=1.563	[V]
19	0.612*VLCD	V0=3.367	V0=3.061	V0=2.449	V0=2.143	V0=1.837	V0=1.531	[V]
20	0.600*VLCD	V0=3.300	V0=3.000	V0=2.400	V0=2.100	V0=1.800	V0=1.500	[V]
21	0.588*VLCD	V0=3.235	V0=2.941	V0=2.353	V0=2.059	V0=1.765	V0=1.471	[V]
22	0.576*VLCD	V0=3.173	V0=2.885	V0=2.308	V0=2.019	V0=1.731	V0=1.442	[V]
23	0.566*VLCD	V0=3.113	V0=2.830	V0=2.264	V0=1.981	V0=1.698	V0=1.415	[V]
24	0.555*VLCD	V0=3.056	V0=2.778	V0=2.222	V0=1.944	V0=1.667	V0=1.389	[V]
25	0.545*VLCD	V0=3.000	V0=2.727	V0=2.182	V0=1.909	V0=1.636	V0=1.364	[V]
26	0.535*VLCD	V0=2.946	V0=2.679	V0=2.143	V0=1.875	V0=1.607	V0=1.339	[V]
27	0.526*VLCD	V0=2.895	V0=2.632	V0=2.105	V0=1.842	V0=1.579	V0=1.316	[V]
28	0.517*VLCD	V0=2.845	V0=2.586	V0=2.069	V0=1.810	V0=1.552	V0=1.293	[V]
29	0.508*VLCD	V0=2.797	V0=2.542	V0=2.034	V0=1.780	V0=1.525	V0=1.271	[V]
30	0.500*VLCD	V0=2.750	V0=2.500	V0=2.000	V0=1.750	V0=1.500	V0=1.250	[V]
31	0.491*VLCD	V0=2.705	V0=2.459	V0=1.967	V0=1.721	V0=1.475	V0=1.230	[V]

Note:

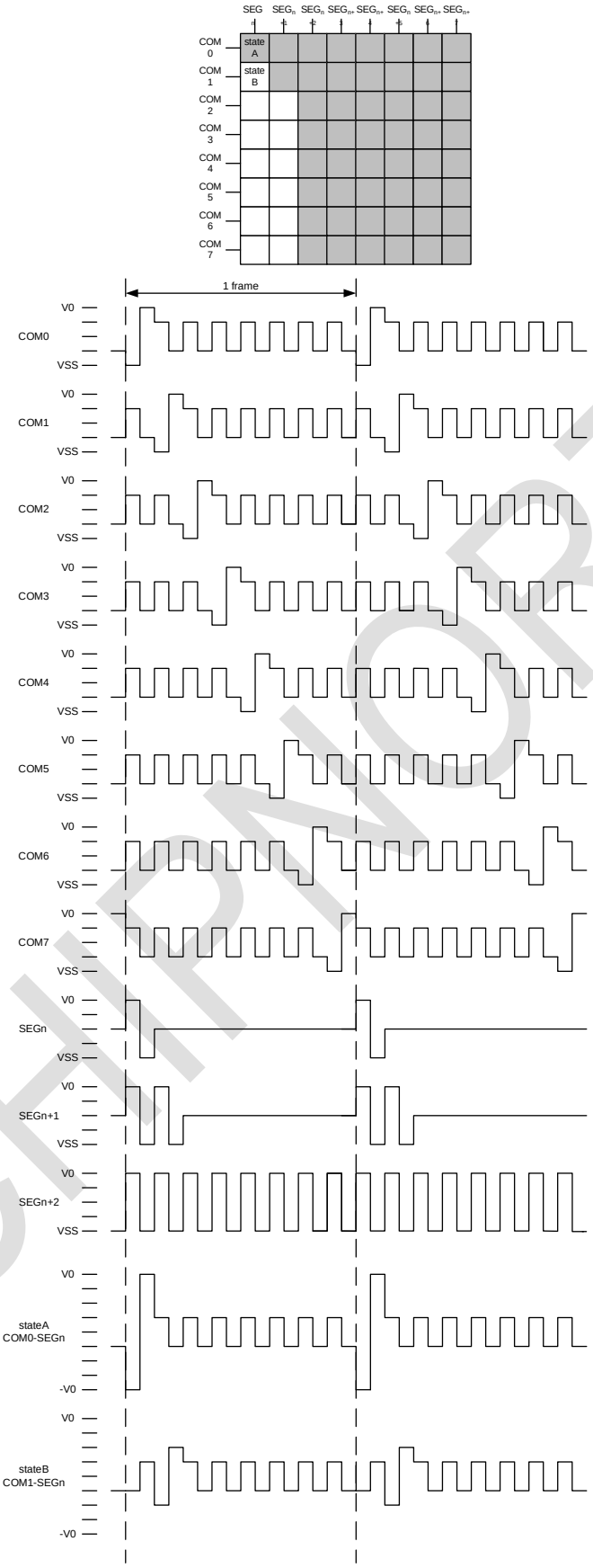
1.The shaded areas are prohibited for setting.

2.VLCD-V0>0.3V

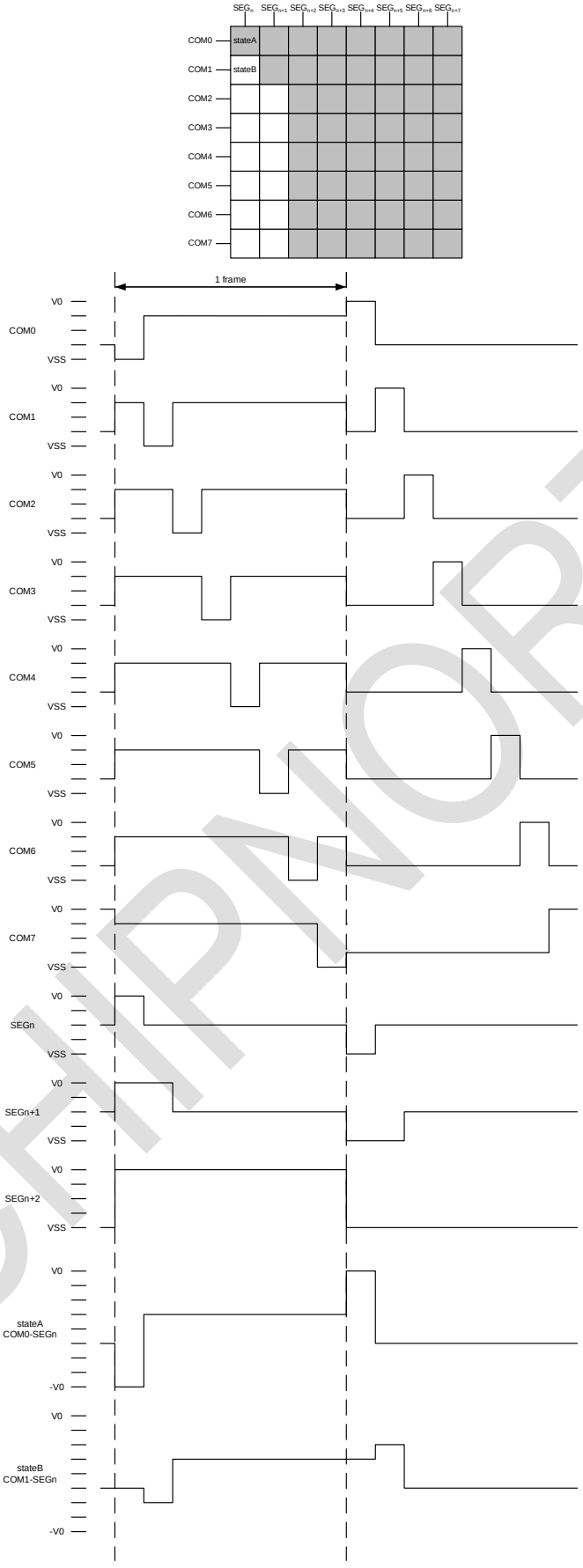
3.V0>2.5V

15 LCD Drive Waveform

（1/4bias,1/8duty）Line inversion mode



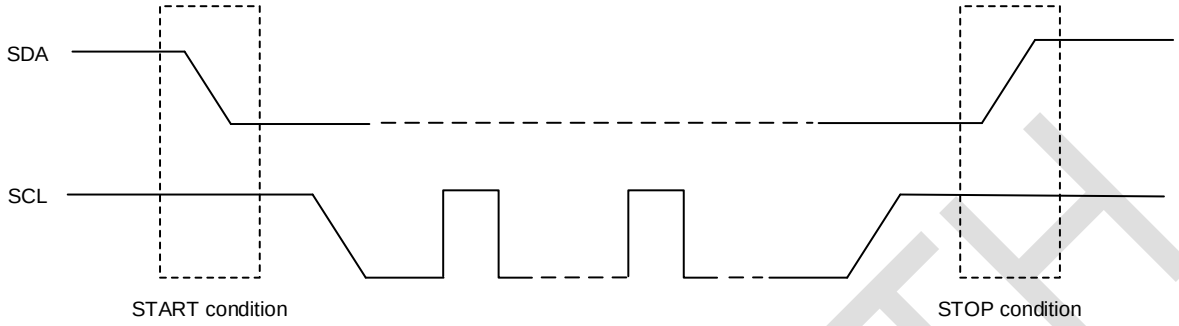
（1/4bias,1/8duty）Frame inversion mode



16 Function Description

16.1 Command and Data Transfer Method

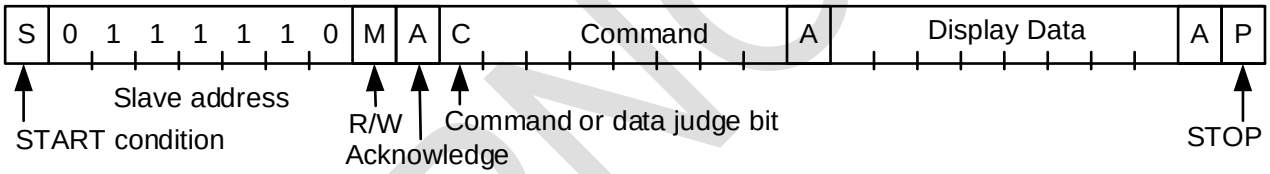
When transmitting commands or data through the 2-wire serial interface, this device must generate “START condition” and “STOP condition” states. When SCL is held high and SDA transitions from a high to a low level, it is considered a “START condition”. When SCL is held high and SDA transitions from a low to a high level, it is considered a “STOP condition”.



Start and Stop Conditions Diagram

Method of how to transfer command and data is shown as follows.

1. Generate “START condition”.
2. Issue Slave address 0x7C.
3. Transfer command.
4. Transfer display data.
5. Generate “STOP condition”.



16.2 Acknowledge

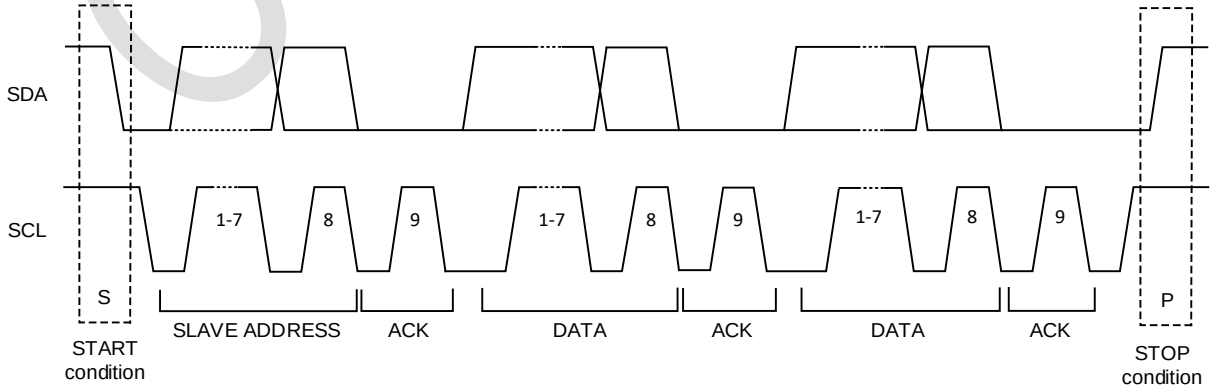
When transfer data, always need Acknowledge.

Data format is 8bits and return Acknowledge after transfer 8bits data.

When SCL 8th= “L” after transfer 8bit data (Slave Address, Command, Display Data), output “L”and open SDA line.

When SCL 9th= “L”, stop output function. (As Output format is NMOS-Open-Drain, can’t output “H” level.)

If no need Acknowledge function, please input “L” level from SCL 8th= “L” to SCL 9th= “L”.

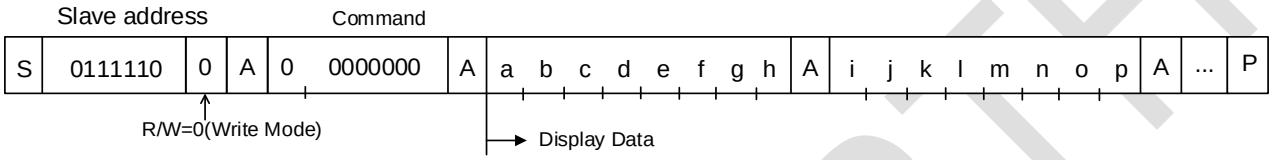


16.3 Command Transfer Method

After generating the “start condition”, send the slave address “01111100”(write mode), and then immediately transmit the command. The most significant bit (MSB), known as the “command or data indicator bit”, defines whether the following byte is a command or data. When the “command or data indicator bit” is set to “1”, the next byte is treated as a command. When the “command or data indicator bit” is set to “0”, the next byte is considered display data.

S	Slave address	A	1	Command	A	1	Command	A	1	Command	A	0	Command	A	Display Data	...	P

CN90C8S35 is equipped with a 280-bit display data RAM (DDRAM), organized as 35×8. When the R/W bit of the address is “0”, it indicates a write data mode. The correspondence between display data and write data, as well as the correspondence between DDRAM data, addresses, and display, is as follows.

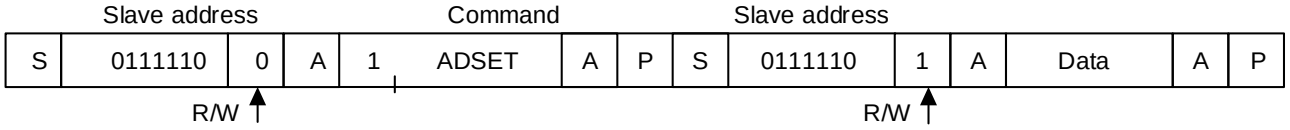


8-bit data is written into the DDRAM. The writing area is specified by the ADSET command, and the address for each 8-bit data automatically increments. Therefore, continuous data transmission can be used to continuously write data into the DDRAM.

BIT	0h	1h	2h	3h	4h	5h	6h	7h	……	21h	22h	
0	a	i										COM0
1	b	j										COM1
2	c	k										COM2
3	d	l										COM3
4	e	m										COM4
5	f	n										COM5
6	g	o										COM6
7	h	p										COM7
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	

16.4 Read Command Register and Transfer Method

CN90C8S35 enters “Read mode” when R/W bit of Slave address is “1".
During Read mode the command registers can be read.
The sequence for the command register read is shown below.



The following register settings can be read in this mode.
Only one register setting can be read at once, after reading register setting, CN90C8S35 will exit from read mode and wait for slave address. If all register setting needs to be read, please make sequence for “REG1” and “REG2”, respectively.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	0	0	RST	EVR[4:0]					23h
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOFF	24h

17 Initialize sequence

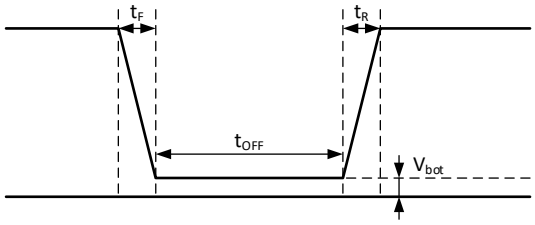
Please follow the sequence below after Power-On to set this device to initial condition. Power on
↓
STOP condition
↓
START condition
↓
Issue Slave address
↓
Execute Software Reset by ICSET command
Each register value and DDRAM address is initialized to their default values.
DDRAM data is random after power on.

18 Working Example

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0 to 5V(Tr=0.1ms)
	↓									
2	wait 100us									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
8	EVRSET	1	1	0	0	0	0	0	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	⋮ ⋮									⋮ ⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	Stop									Stop condition
	↓									
12	Start									Start condition
13	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display ON

19 Caution in P.O.R circuit use

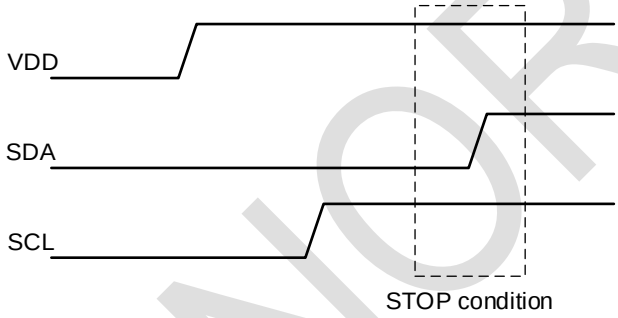
This device has “P.O.R.” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.
Please set power up conditions to meet the recommended t_R, t_F, t_{OFF}, and V_{bot} spec below in order to ensure P.O.R. operation.



Recommended condition of t_R, t_F, t_{OFF}, V_{bot} (Ta=25 ºC)			
t_R	t_F	t_{OFF}	V_{bot}
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

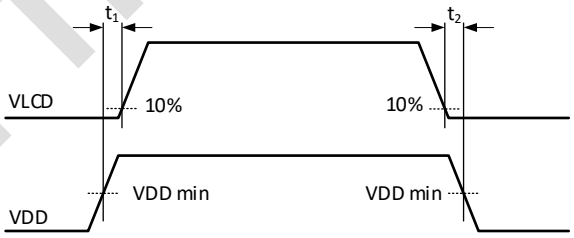
If it is difficult to meet above conditions, execute the following sequence after Power-On.

1) STOP condition
2) START condition.
3) Issue Slave address.
4) Execute Software Reset (ICSET) command.



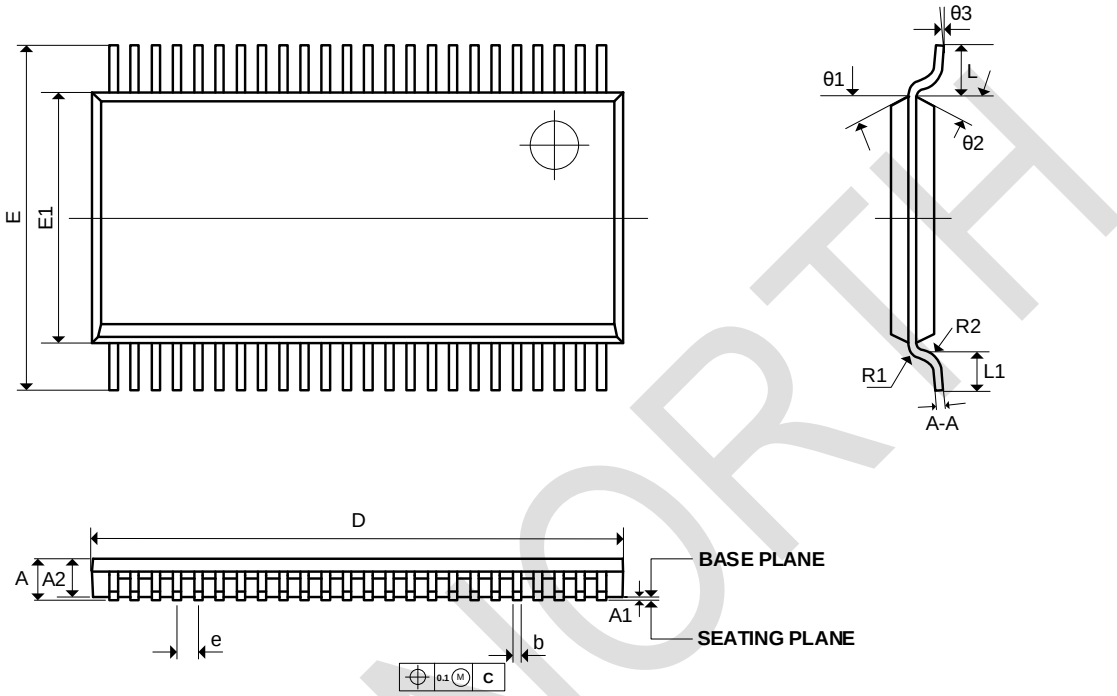
20 Power Up Sequence and Power Down Sequence

To prevent incorrect display, malfunction and abnormal current,
VDD must be turned on before VLCD In power up sequence.
VDD must be turned off after VLCD In power down sequence.
Please satisfies t_1>0ns, t_2>0ns.



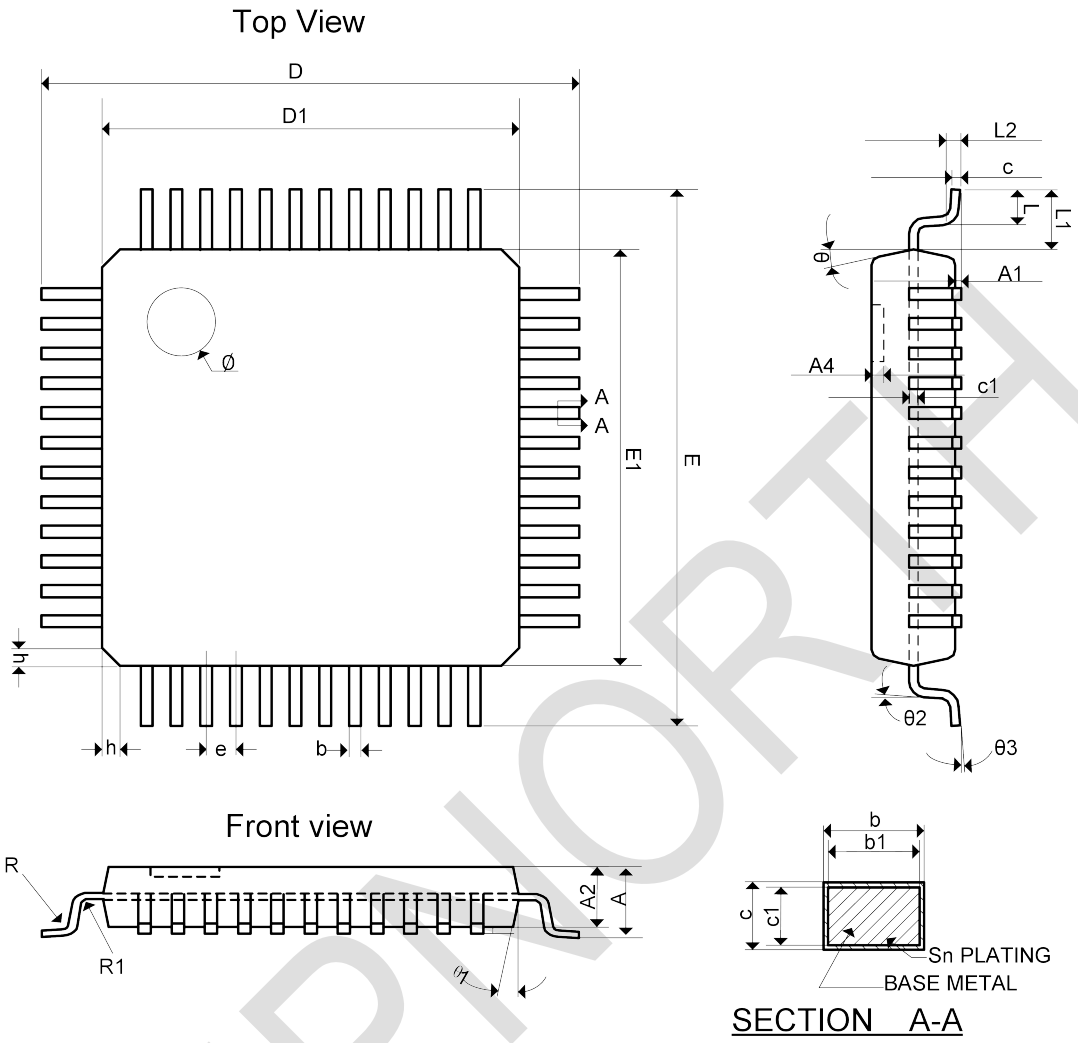
21 Package Information

TSSOP48



SIZE / SYMBOL	MIN (mm)	MAX (mm)	SIZE / SYMBOL	MIN (mm)	MAX (mm)
A		1.2	e	0.5	
A1	0.03	0.13	b	0.17	0.27
A2	0.824	1.024	R1	0.22TYP	
E	7.9	8.3	R2	0.22TYP	
E1	6	6.2	A-A	0.12	0.22
D	12.4	12.6	θ1	12°TYP	
L		1	θ2	12°TYP	
L1	0.35	0.65	θ3	0°	8°

LQFP48



	SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)		SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)
TOTAL THICKNESS	A	-	-	1.60	LEAD PITCH	e	0.50BSC		
STAND OFF	A1	0.05	0.10	0.20	CHAMFER	h	0.20	0.30	0.40
BODY THICKNESS	A2	1.35	1.40	1.45	FOOT LENGTH	L	0.45	0.65	0.75
UP BODY THICKNESS	A3	0.64BSC			LEAD LENGTH	L1	1.00BSC		
THIMBLE DEPTH	A4	0.10	0.20	0.30	MEASURE POINT	L2	0.25BSC		
LEAD WIDTH	b	0.17	0.225	0.28	R RADIUS	R	0.15 REF		
LEAD WIDTH	b1	0.20BSC			R1 RADIUS	R1	0.12 REF		
L/F THICKNESS	c	0.127	-	0.16	ANGLE FOR MOLD	θ	12° TYP		
L/F THICKNESS	c1	0.107	0.127	0.147	ANGLE FOR MOLD	θ1	12° TYP		
TOTAL SIZE X	D	8.80	9.00	9.20	ANGLE FOR LEAD	θ2	4° TYP		
BODY SIZE X	D1	6.90	7.00	7.10	ANGLE FOR FOOT	θ3	0° ~8°		
TOTAL SIZE Y	E	8.80	9.00	9.20	THIMBLE DIAMETER	Ø	1.10	1.20	1.30
BODY SIZE Y	E1	6.90	7.00	7.10					

22 Important Statement

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23 Revision History

Date	Version	Revision Notes
2021/07/10	R1.0	Official Release
2022/04/05	R1.3	Add LQFP48 package
2023/03/08	R1.4	Update VLCD description
2024/05/14	R1.5	Update order information, the pin description diagram, typical application circuit diagram, structure diagram, time sequence diagram, start stop condition diagram, DDRAM diagram, EVR comparison table, workflow table, the command and data transmission method description
2024/09/29	R1.6	Update package information
2024/11/22	R1.7	Add “4Marking”, Update Block Diagram
2025/01/15	R1.8	Update the format
2025/02/28	R1.9	Update absolute maximum ratings
2025/09/05	R2.0	Update the LCD driver waveform, Order Information, the diagram in Command Transfer Method
2026/08/24	R2.1	Update the block diagram, diagram in Read Command Register and Transfer Method, SDA setup time and SDA hold time, typical application diagram