4COM Segment type LCD Driver,6uA typ.

1 Description

The CN9103C4S48 is a segment-type LCD driver chip with a duty cycle of 1/4, capable of driving up to 192 segments. This device incorporates a low-power design, enabling it to achieve ultra-low power consumption and reduce power loss from the power supply.

2 Features

- Fixed 1/4 duty mode, Up to 192 dots
- Low power consumption design, 6uA current at typical condition
- Built-in OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Interface: 2 line serial I2C
- Compatible with TTL/CMOS
- High EMC immunity

3 Applications

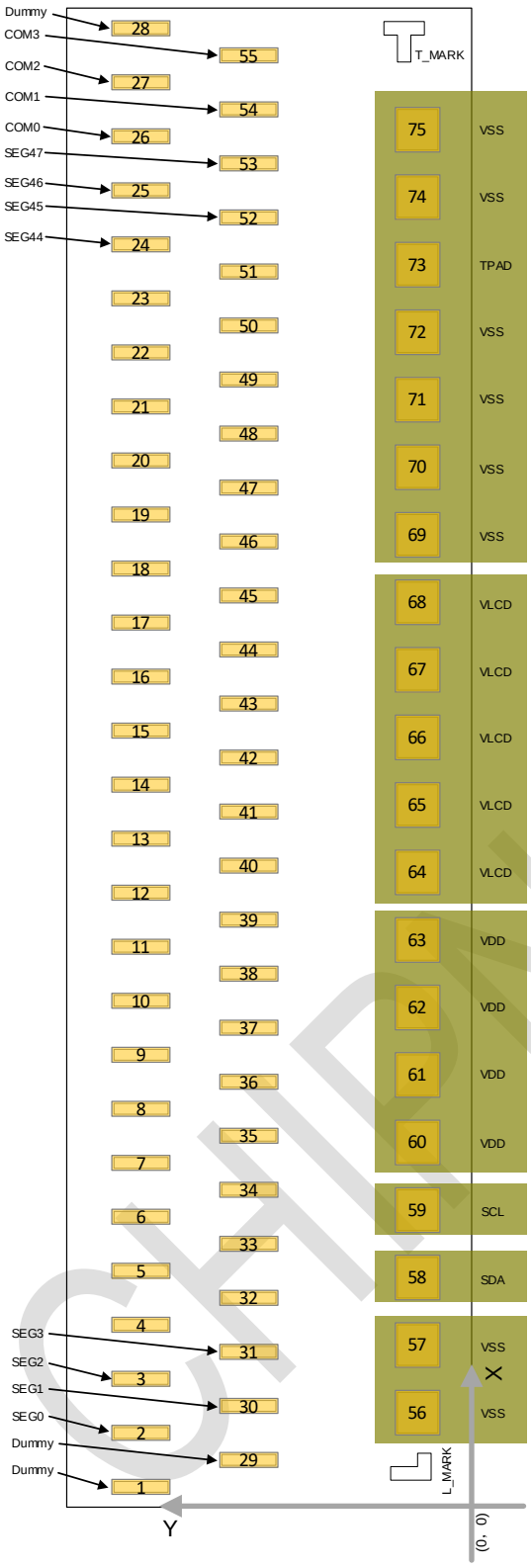
- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

4 Order Information

Product Number	Package	Quantity
CN9103C4S48	COG	252/Tray

5 PAD Description

Name	I/O	Function
SDA	I/O	2-line serial data input and output
SCL	I	2-line serial clock input
VSS	I	GND
VDD	I	Power
VLCD	I	Set LCD bias voltage. It can be directly tied to VDD, and then you can adjust the internal LCD bias voltage by setting the register EVR[3:0].
TPAD	I	Should be directly tied to GND
SEG0~SEG47	O	SEGMENT driver output for LCD
COM0~COM3	O	COMMON driver output for LCD



Die Thickness: 300um

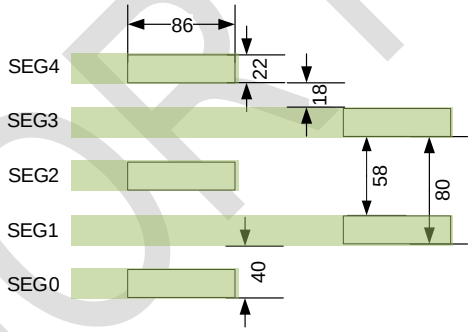
Die Size(without scribe lane): 2220um X 600um

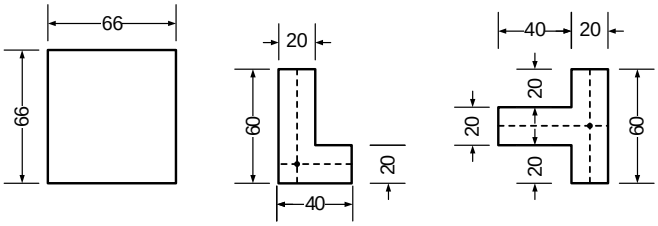
Bump Hight: 9um±2um

SEG Bump Width: 22um

SEG Bump Space: 18um

SEG Bump Pitch: 40um



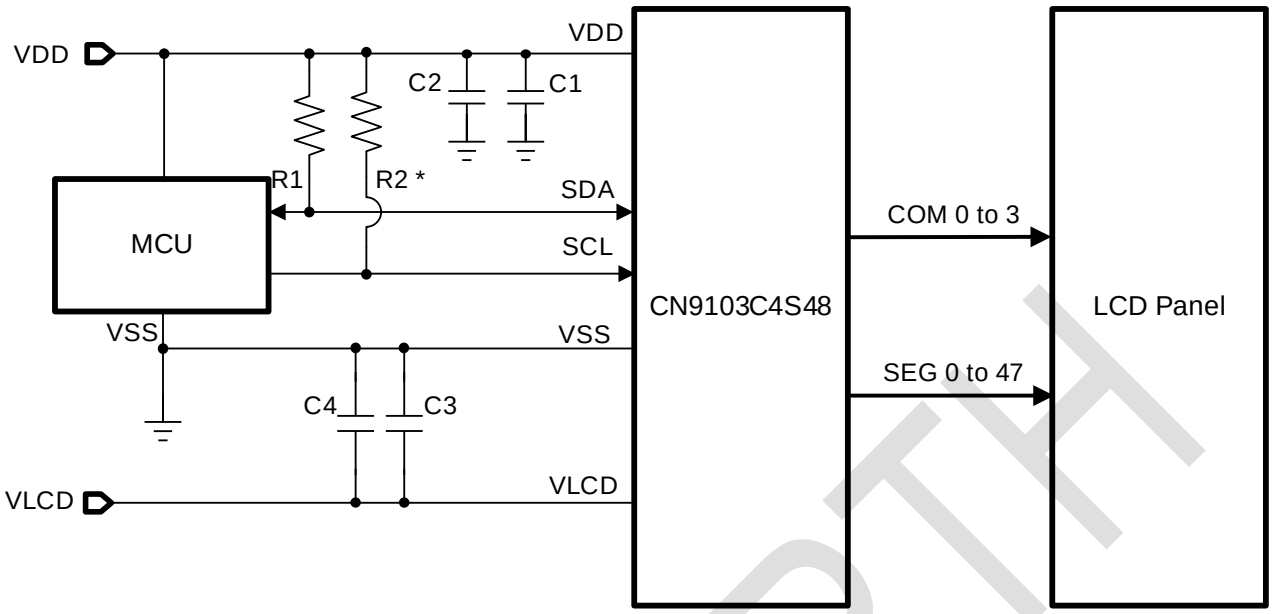


6 PAD Coordinates for COG

UNIT： μm

No	Name	X	Y	No	Name	X	Y
1	Dummy	30	490	39	SEG19	870	330
2	SEG0	110	490	40	SEG21	950	330
3	SEG2	190	490	41	SEG23	1030	330
4	SEG4	270	490	42	SEG25	1110	330
5	SEG6	350	490	43	SEG27	1190	330
6	SEG8	430	490	44	SEG29	1270	330
7	SEG10	510	490	45	SEG31	1350	330
8	SEG12	590	490	46	SEG33	1430	330
9	SEG14	670	490	47	SEG35	1510	330
10	SEG16	750	490	48	SEG37	1590	330
11	SEG18	830	490	49	SEG39	1670	330
12	SEG20	910	490	50	SEG41	1750	330
13	SEG22	990	490	51	SEG43	1830	330
14	SEG24	1070	490	52	SEG45	1910	330
15	SEG26	1150	490	53	SEG47	1990	330
16	SEG28	1230	490	54	COM1	2070	330
17	SEG30	1310	490	55	COM3	2150	330
18	SEG32	1390	490	56	VSS	140	80
19	SEG34	1470	490	57	VSS	240	80
20	SEG36	1550	490	58	SDA	340	80
21	SEG38	1630	490	59	SCL	440	80
22	SEG40	1710	490	60	VDD	540	80
23	SEG42	1790	490	61	VDD	640	80
24	SEG44	1870	490	62	VDD	740	80
25	SEG46	1950	490	63	VDD	840	80
26	COM0	2030	490	64	VLCD	940	80
27	COM2	2110	490	65	VLCD	1040	80
28	Dummy	2190	490	66	VLCD	1140	80
29	Dummy	70	330	67	VLCD	1240	80
30	SEG1	150	330	68	VLCD	1340	80
31	SEG3	230	330	69	VSS	1440	80
32	SEG5	310	330	70	VSS	1540	80
33	SEG7	390	330	71	VSS	1640	80
34	SEG9	470	330	72	VSS	1740	80
35	SEG11	550	330	73	TPAD	1840	80
36	SEG13	630	330	74	VSS	1940	80
37	SEG15	710	330	75	VSS	2040	80
38	SEG17	790	330	76	T_Mark	2170	85
				77	L_Mark	50	65

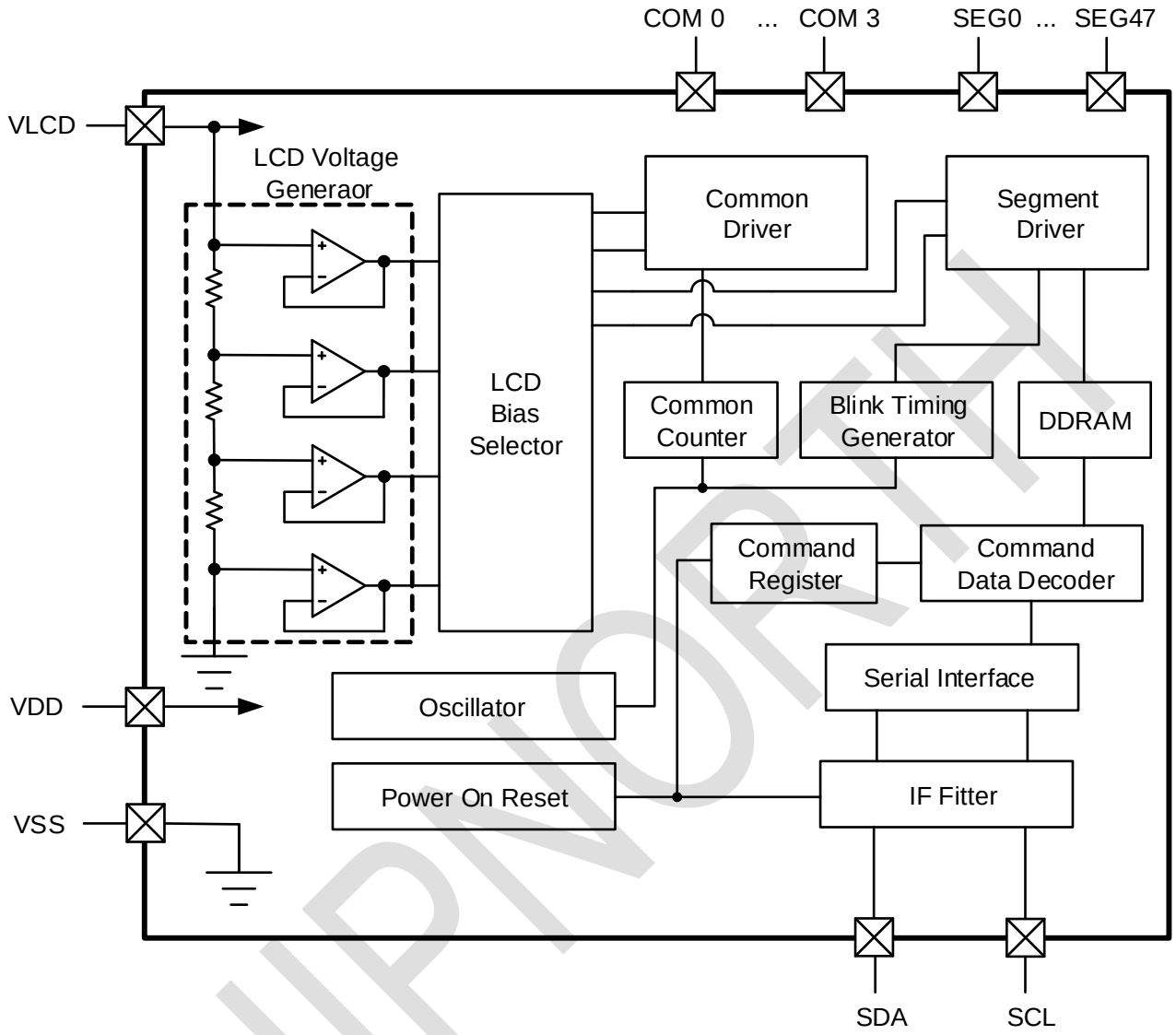
7 Typical Application



Note: 1.* R2 is optional.

2. C1 and C3 are recommended to be 0.1 uF. C2 and C4 are recommended to be 10 uF. The capacitors shall be placed close to the IC pins during layout.

8 Block Diagram



9 Specifications

9.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Rating	Remarks
Power Supply Voltage	V_{DD}	-0.3~+6.5	V	Power supply
Power Supply Voltage	V_{LCD}	-0.3 to +6.5	V	LCD drive voltage
Input voltage range	V_{IN}	-0.3 to V_{DD}+0.3	V	
Soldering Temperature	T_{lead}	260（soldering，10s）	°C	
Operational temperature range	T_{opr}	-40 to 125	°C	
Storage temperature range	T_{stg}	-55 to 150	°C	

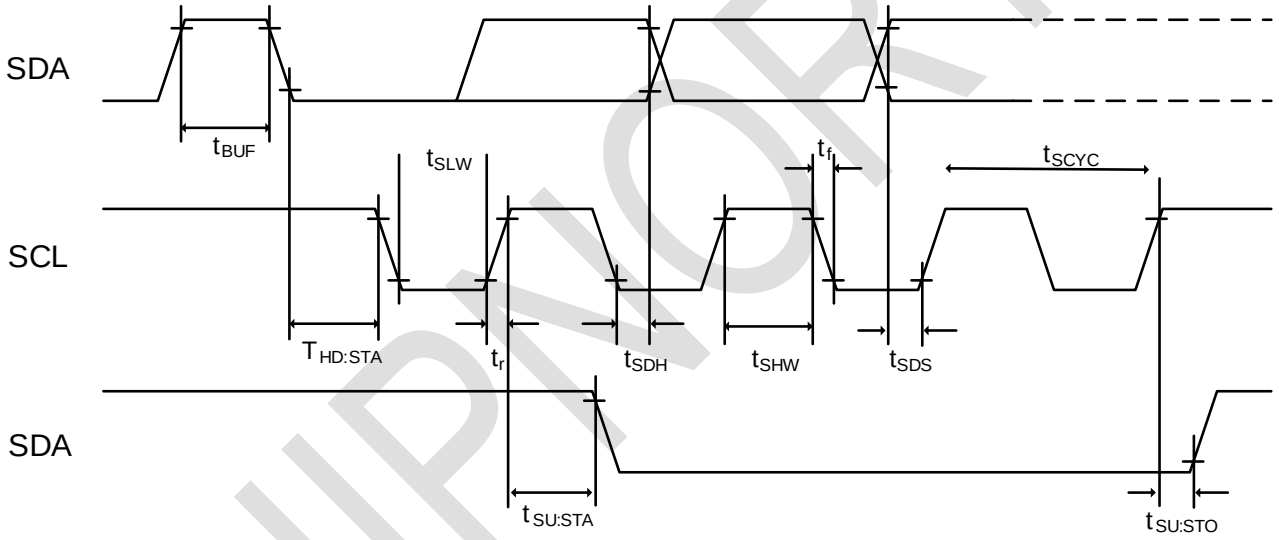
9.2 Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD Power Range	V_{DD}		2.5	-	5.5	V
VLCD Power Range	V_{LCD}	LCD drive voltage	2.5	-	5.5	V
“H” Level Input Voltage	V_{IH}		1.4	-	V_{DD}	V
“L” Level Input Voltage	V_{IL}		V_{SS}	-	0.4	V
SDA "L" Level Output Voltage	V_{OL_sda}	I_{Load}=-3mA Without the consideration of ITO resistance on COG panel.	0	-	0.4	V
COM ON Resistance	R_{ON}	I_{Load}=±10uA	-	3	-	kΩ
SEG ON Resistance	R_{ON}	I_{Load}=±10uA	-	3	-	kΩ
Standby Current	I_{DD1}	Display off, Oscillation off	-	-	1	uA
Operating Current	I_{DD}	VDD=3.3V, VLCD=3.3V,Ta=25℃, SR=Power save mode 1, Frame inversion, FR=72Hz, with an LCD panel load.	-	3	-	uA
Operating Current	I_{VLCD}	VDD=3.3V, VLCD=3.3V,Ta=25℃, SR=Power save mode 1, Frame inversion, FR=72Hz, with an LCD panel load.	-	3	-	uA
Frame Frequency	F_{clk}	FR=72Hz setting	-	72	-	Hz

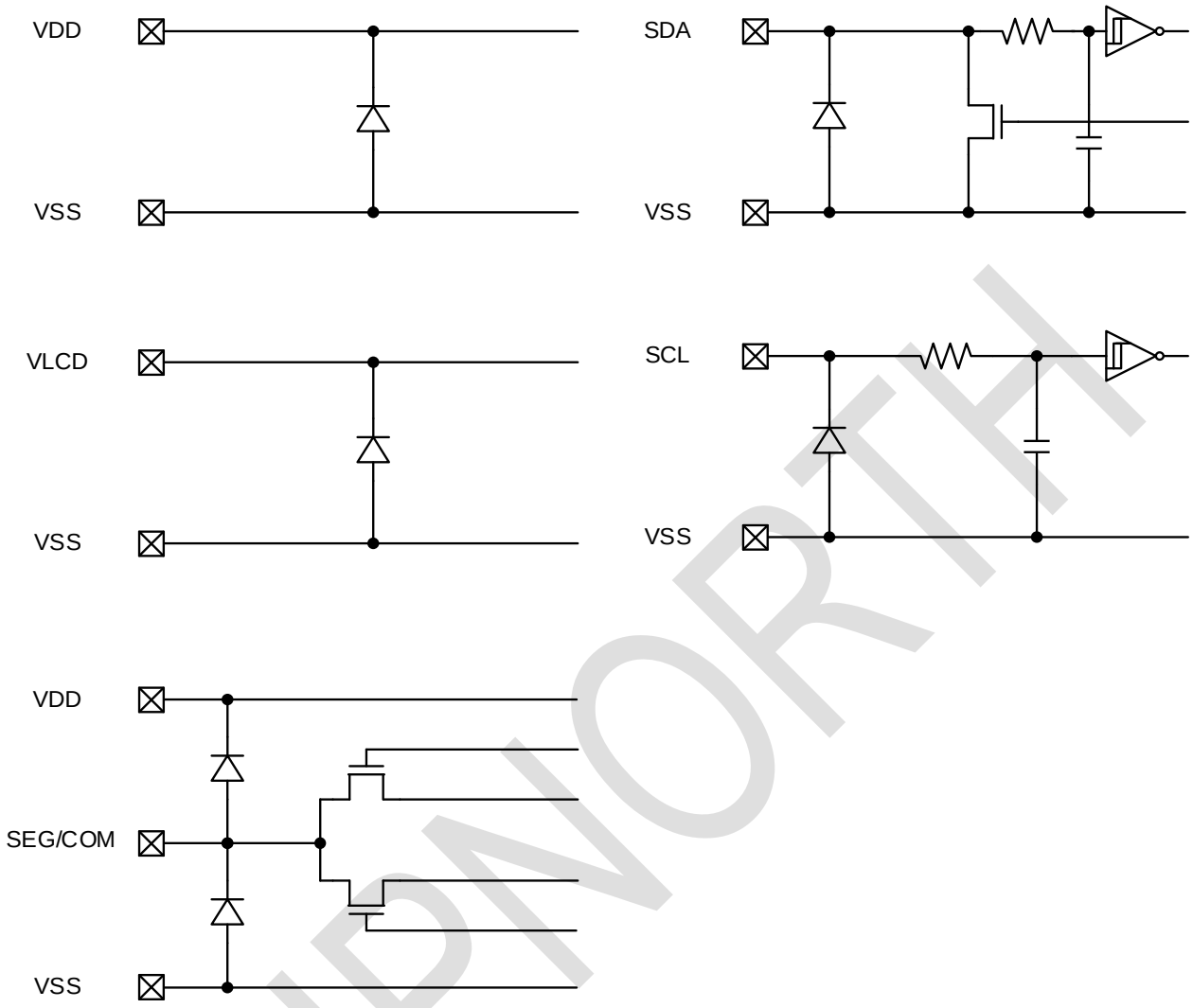
9.3 MPU Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Rise Time	t_r		-	-	0.3	μs
Input Fall Time	t_f		-	-	0.3	μs
SCL Cycle Time	t_{CYC}		2.5	-	-	μs
“H” Level SCL Pulse Width	t_{HW}		0.6	-	-	μs
“L” Level SCL Pulse Width	t_{LW}		1.2	-	-	μs
SDA Setup Time	t_{SDS}		100	-	-	ns
SDA Hold Time	t_{SDH}		100	-	-	ns
Bus Free Time	t_{BUF}		1.3	-	-	μs
START Condition Hold Time	$t_{HD;STA}$		0.6	-	-	μs
START Condition Setup Time	$t_{SU;STA}$		0.6	-	-	μs
STOP Condition Setup Time	$t_{SU;STO}$		0.6	-	-	μs



2-line serial interface timing

10 Equivalent circuit of input and output



11 Command Registers Description

	D7	D6	D5	D4	D3	D2	D1	D0
ADSET	**C**	**0**	**0**	P[4:0]				
DISCTL	**C**	**0**	**1**	FR[1:0]		LF	SR[1:0]	
MODSET	**C**	**1**	**0**	ULP	EN	/	/	/
EVRSET	**C**	**1**	**1**	**0**	**0**	EVR[2:0]		
ICSET	**C**	**1**	**1**	**0**	**1**	P[5]	RST	P[6]
BLKCTL	**C**	**1**	**1**	**1**	**0**	BF[2:0]		
APCTL	**C**	**1**	**1**	**1**	**1**	EVR[3]	AON	AOFF

Name	Default	Description
P[6:0]	0000000	DDRAM Address. In the write mode, the range of address P [6:0] can be set as 0~2F(Hex). In the read mode, the range of address P [6:0] can be set as 0~2F, 30~32(Hex). Don't specify another address, otherwise address will be set to "0000000". Note: The P[5] and P[6] are in the command 'ICSET'.
FR[1:0]	00	Set Frame Frequency for Power Saving. 00, 72Hz, Normal Mode 01, 96Hz Operating Mode1 10, 49Hz, Operating Mode 2 11, 144Hz, Operating Mode 3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value 11, *1.8, High Power Mode
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	0: disable all blocks on-chip, all com/seg pin will be pulled to GND. 1: enable
EVR[3:0]	0000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * VLCD 0001, 0.975 * VLCD 0010, 0.950 * VLCD 0011, 0.925 * VLCD 0100, 0.900 * VLCD 0101, 0.875 * VLCD 0110, 0.850 * VLCD 0111, 0.825 * VLCD 1000, 0.800 * VLCD 1001, 0.775 * VLCD 1010, 0.750 * VLCD 1011, 0.725 * VLCD 1100, 0.700 * VLCD 1101, 0.675 * VLCD 1110, 0.650 * VLCD 1111, 0.625 * VLCD Note: The bit EVR[3] is in the command 'APCTL'.
RST	0	Set '1' to reset all the registers in this table, but it won't reset the display data in the DDRAM.
BF[2:0]	000	Config the blink frequency. 000, No blink.

		001, 0.5Hz 010, 1Hz 011, 2Hz 100~111, 0.25Hz
AON: AOFF	00	Config the pixel display. 00, All pixels are ON/OFF depending on the data in the display DDRAM. 01, All pixels are OFF regardless of DDRAM data. 10, All pixels are ON regardless of DDRAM data. 11, All pixels are OFF regardless of DDRAM data, the same as '01'.

12 Function Description

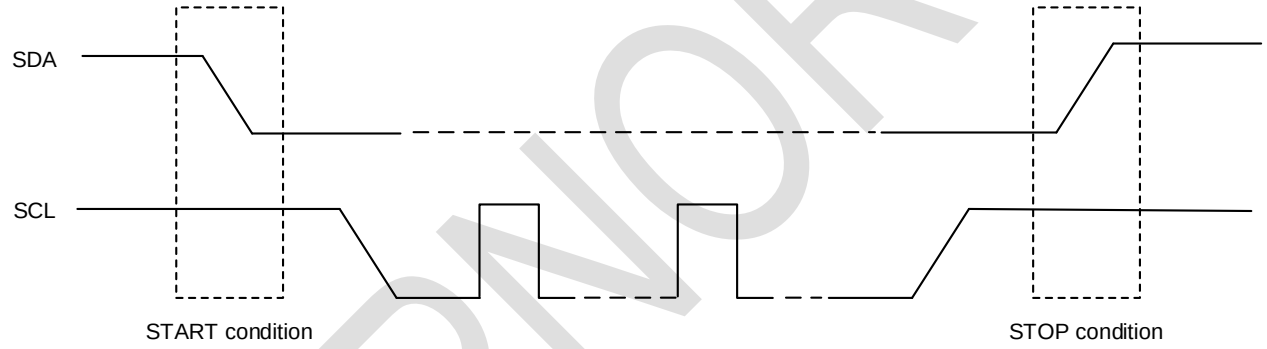
12.1 Command and Data Transfer Method

This Device is transfer data by 2-line serial interface.

When input command or data by 2-line serial interface, it must be generated the state of "START condition" and "STOP condition".

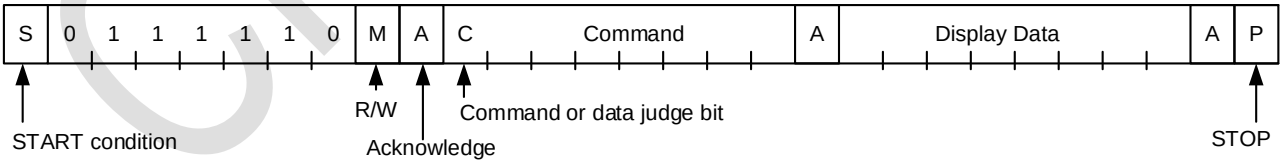
When set SDA "H"→"L" in SCL="H", it become "START condition".

When set SDA "L"→"H" in SCL="H", it become "STOP condition"



START condition and STOP condition.

1. Generate "START condition".
2. Issue Slave address 0x7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"

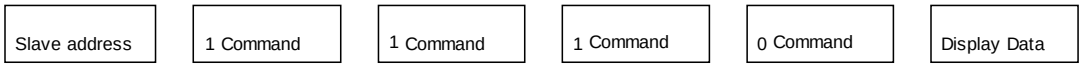


Issue the Slave Address ("01111100" for Write Mode or "01111101" for Read Mode) after the "START condition" is generated. Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation to be done is Write or Read operation.

The MSB (command or data judgment bit) defines if the succeeding byte is a command or data.

When "command or data judgment bit" ='1', the next byte is a command.

When "command or data judgment bit" ='0', the next byte is display data.



Once it enters display data transfer condition, it cannot input any command.

To input command again, please generate the “START condition” again.

If “START condition” or “STOP condition” is inputted in the middle of command transmission, the command will be cancelled. If the Slave address is continuously inputted following “START condition”, it will be in command input condition.

Please input “Slave Address” in the first data transmission after “START condition”.

When Slave Address cannot be recognized in the first data transmission, Acknowledge does not return and the next transmission will be invalid. When data transmission is in invalid status and the “START condition” is transmitted again, it will return to valid status.

Note: Please confirm that MPU Interface characteristic of Input rise/fall time and setup/hold time in transferring command and data meet the AC specifications. Refer to “MPU Interface Characteristics”.

12.2 Write Display Data and Transfer Method

Set R/W bit to ‘0’ to come into write mode.

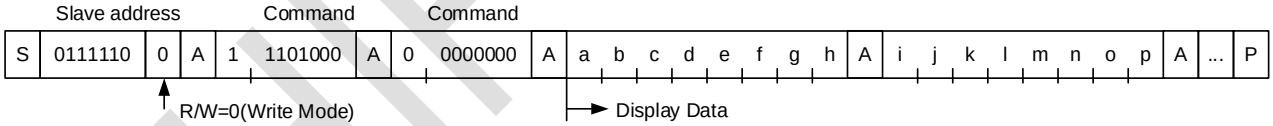
This device has Display Data RAM (DDRAM) of 48×4=192bit.

DDRAM address

BIT	00h	01h	02h	03h	04h	05h	06h	07h	……	2Dh	2Eh	2Fh	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	……	SEG45	SEG46	SEG47	

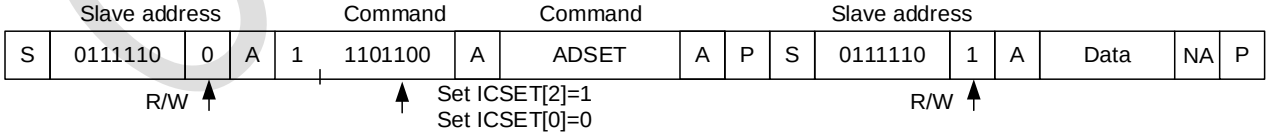
8bit data will be stored in DDRAM. The address to be written is the address specified by Address set command (ADSET), and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.



12.3 Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data read sequence.

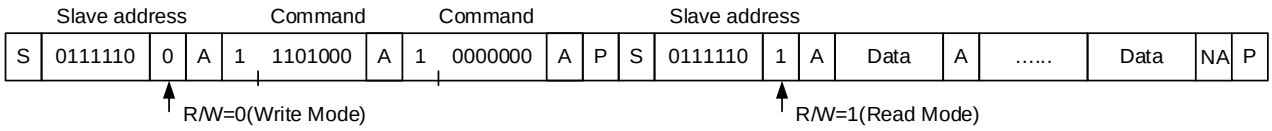


The command register addresses are described below. The following register settings can be read in this mode.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			30H
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOFF	31H
REG3	/	/	/	ULP	EVR[3:0]				32H

12.4 Read Display Data and Transfer Method

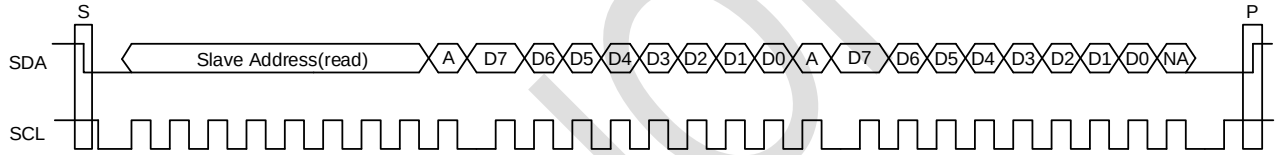
The read mode sequence is shown below.



During read mode, the display data can be read from the DDRAM through the SDA line. The data is outputted serially with SCL input. A write sequence is done first to identify the DDRAM address to be accessed. Then a “START condition” and a “STOP condition” are transmitted before entering the actual reading of DDRAM data and the Slave Address follows. The display data is outputted continuously afterwards. If no DDRAM address was specified right before the DDRAM read, the output during read mode will be from the current DDRAM address.

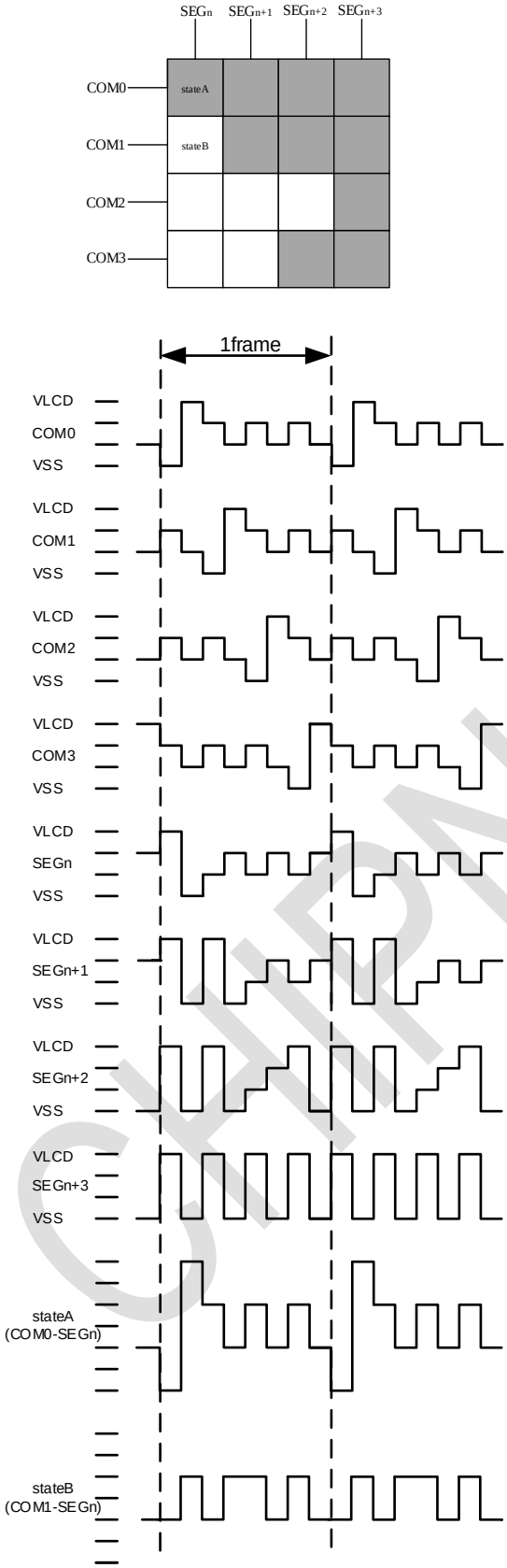
The DDRAM address will increment after every 8-bits of output data. An Acknowledge after every 8-bit of data outputted should be received from the master receiver. This will signal the device that it should continue to output the display data and increment the address. When Non-Acknowledge is received, the device will release the SDA line and the master can then transmit the “STOP condition”. The read mode will be finished once the “STOP condition” is received.

An example of the display data read sequence is shown below.

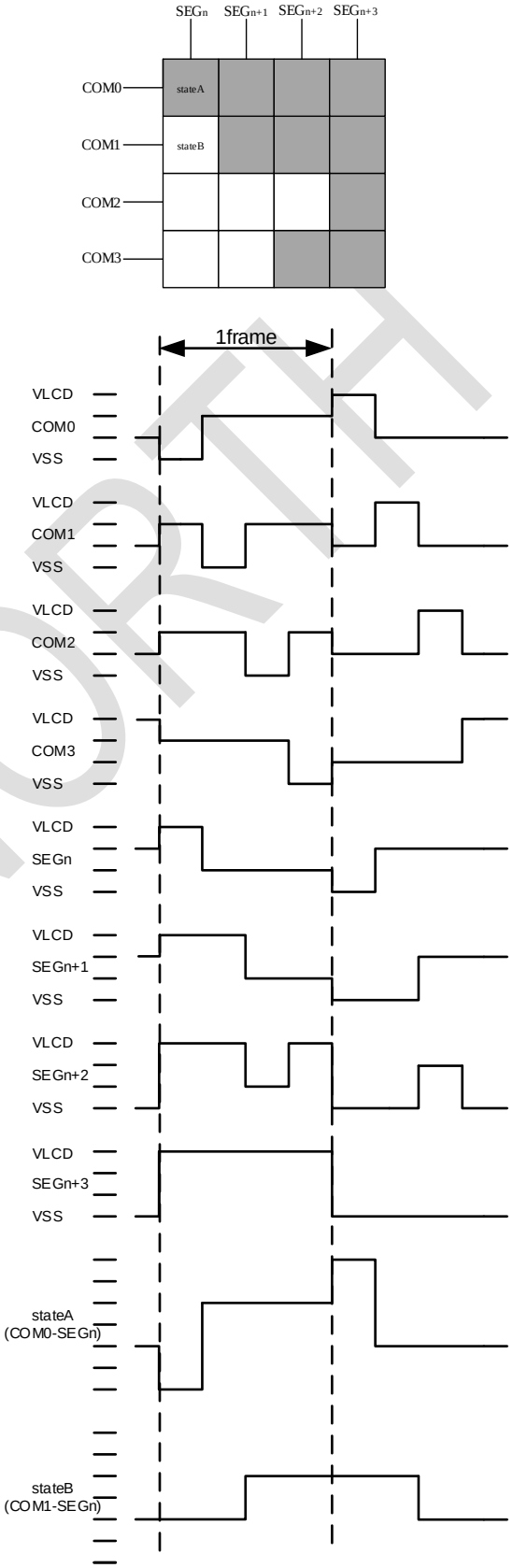


12.5 LCD Driving Waveform

Line Inversion Mode



Frame Inversion Mode



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14 Revision History

Date	Version	Revision Notes
2025/10/16	R1.0	Official Release
2026/08/07	R1.1	Update the block diagram, read mode sequence diagrams, order information and typical application diagram