Bi-direction Relay Driver 4.4~30V
Peak current limit protection:3.5A

1 Description

CN8032 is a bi-direction relay driver circuit, used to control magnetic bi-direction relays. With high output current capability, ultra-low power consumption, it can be widely used in intelligent electro-meter and other related fields.

CN8032 is available in SOT23-6 and SOP-8 package.

2 Features

- Wide power range: 4.4V to 30V
- 3.5A overcurrent protection
- 3.2uA standby mode current
- Low MOSFET on-resistance: Rhs = 0.45Ω, Rls = 0.25Ω
- Back EMF protection
- Suitable for a wide range of MCU control logic
- Input logic hysteresis
- Thermal shutdown

3 Applications

- Smart Circuit Breaker
- Smart Lock
- Smart water/gas meters

4 Ordering information

Product Number	Package	Quantity/Tape
CN8032SHR	SOP-8	4000/ Tape
CN8032ASHR	SOP-8	4000/ Tape
CN8032BSHR	SOP-8	4000/ Tape
CN8032CSHR	SOP-8	4000/ Tape
CN8032TER	SOT23-6	3000/ Tape

5 Marking

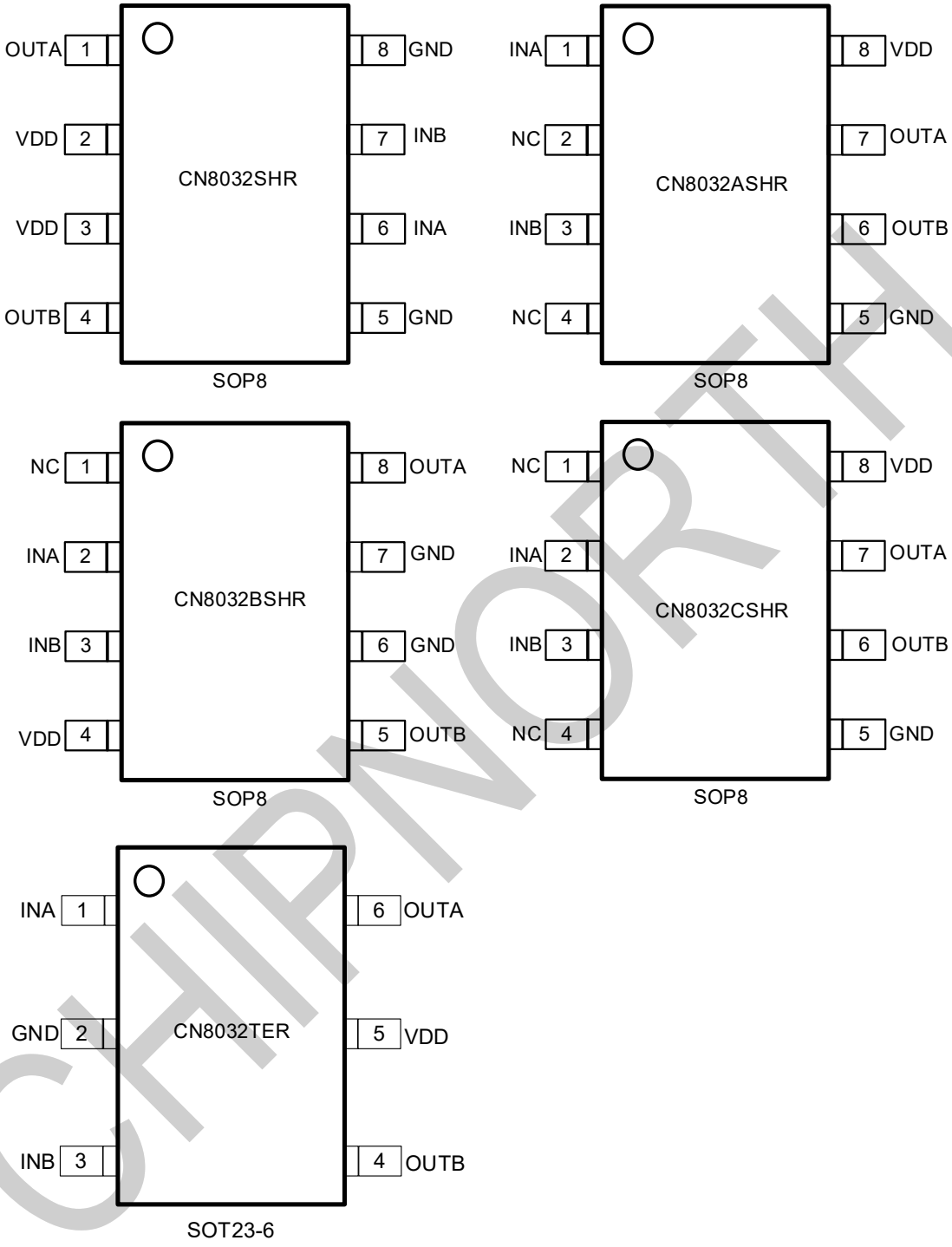
Product Number	Marking
CN8032SHR	CN8032 YYWW
CN8032ASHR	CN8032A YYWW
CN8032BSHR	CN8032B YYWW
CN8032CSHR	CN8032C YYWW
CN8032TER	CN8032 YYWW

Note: YY=Year WW=Week.

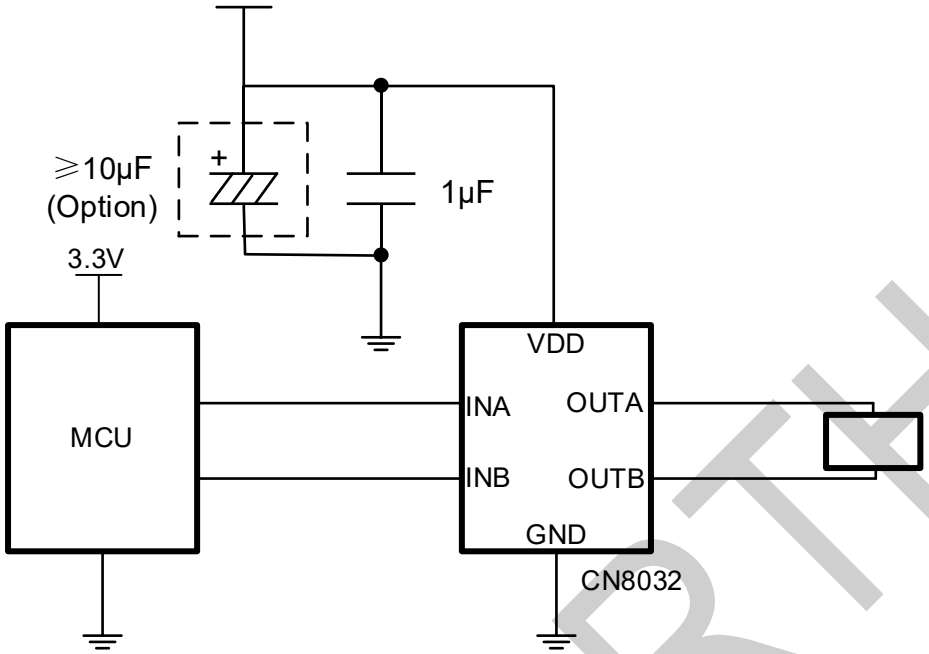
Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances.If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

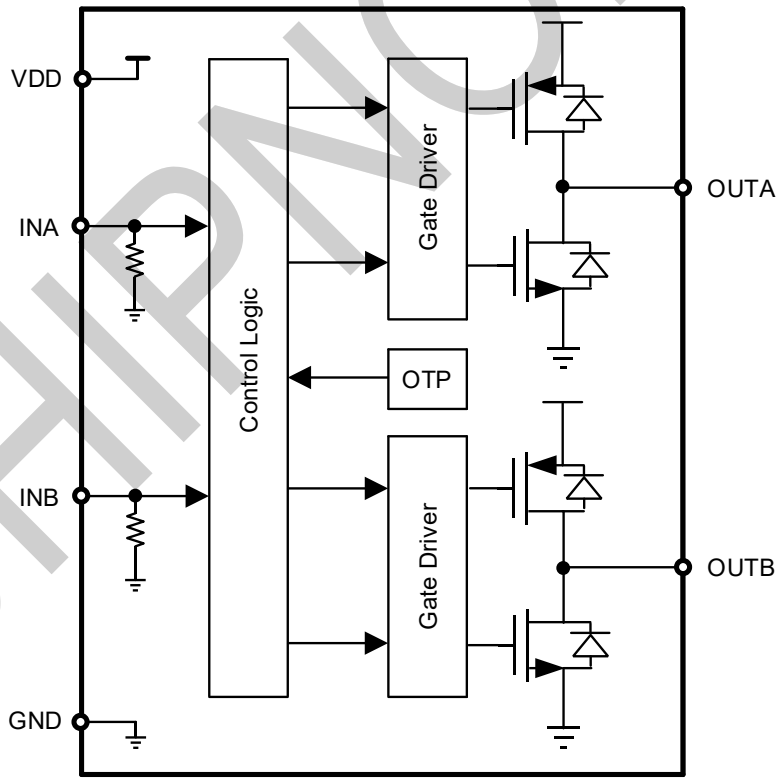
6 Pinout



7 Typical Application



8 Block Diagram



9 Logic Function Table

INA	INB	OUTA	OUTB
0	0	Hi-z	Hi-z
0	1	0	1
1	0	1	0
1	1	0	0

10 Pin Descriptions

CN8032 SHR	CN8032 ASHR	CN8032 BSHR	CN8032 CSHR	CN8032 TER	Pin Name	Descriptions
1	7	8	7	6	OUTA	Output, connect this pin to the relay coils.
2、3	8	4	8	5	VDD	Supply Voltage. A capacitor is required to prevent large voltage spikes.
4	6	5	6	4	OUTB	Output, connect this pin to the Relay coils.
5、8	5	6、7	5	2	GND	GND.
6	1	2	2	1	INA	Logic input with a 1.2M internal pull-down resistor.
7	3	3	3	3	INB	Logic input with a 1.2M internal pull-down resistor.
/	2、4	1	1、4	/	NC	Recommended to be connected to GND.

11 Specifications

11.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
VDD Supply Voltage Range	VDD	-0.4 ~ +37	V
Output Pin Voltage Range	V_{OUTA}、V_{OUTB}	-0.4 ~ +37	V
Input Pin Voltage Range	V_{INA}、V_{INB}	-0.4 ~ 6.6	V
Storage Temperature Range	T_{STG}	-55~150	°C
Lead Temperature	T_{LEAD}	260（soldering，10s）	°C

11.2 ESD Ratings

Discharge mode	Standard	Value	Units
HBM	JEDECJS-001-2023	±8000	V
CDM	JEDECJS-002-2022	±2000	V
Latch up	JESD78F.02-2023	±800	mA

11.3 Recommended Operating Range

Parameter	Symbol	Condition		Min.	Max.	Units
VDD Voltage Range	VDD			4.4	30	V
Input Capacitor	CIN			1		uF
Drive capability	ILOAD	SOP8 （TA=25℃）	Continuous load		1.1	A
			a pulse width of 120 ms and a period of 1 s		2.4	A
			a pulse width of 44 ms and a period of 1 s		3.2	A
		SOT23-6 （TA=25℃）	Continuous load		1	A
			a pulse width of 120 ms and a period of 1 s		2.3	A
			a pulse width of 40 ms and a period of 1 s		3.2	A
Operating Temperature	T_A			-40	105	°C

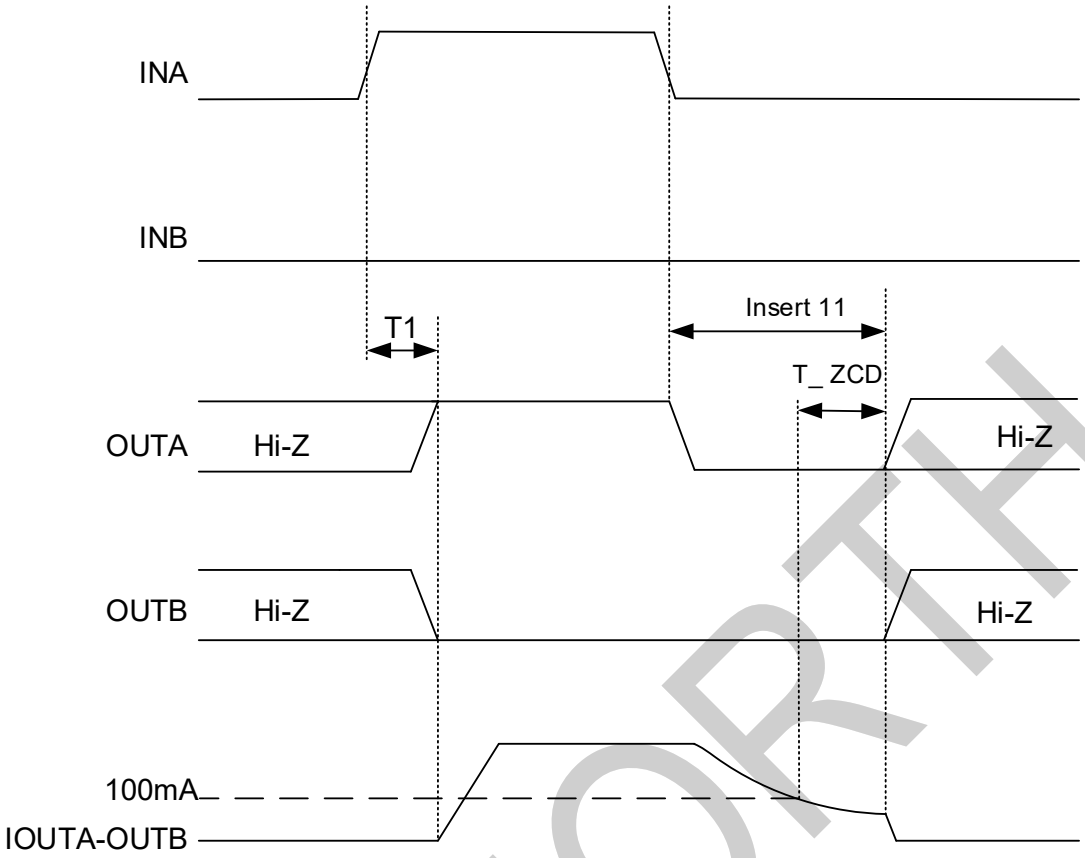
11.4 Thermal Information

Parameter	Package	Value	Unit
θ_{JA}	SOP-8	110	°C/W
	SOT23-6	120	°C/W

11.5 Electrical Characteristics

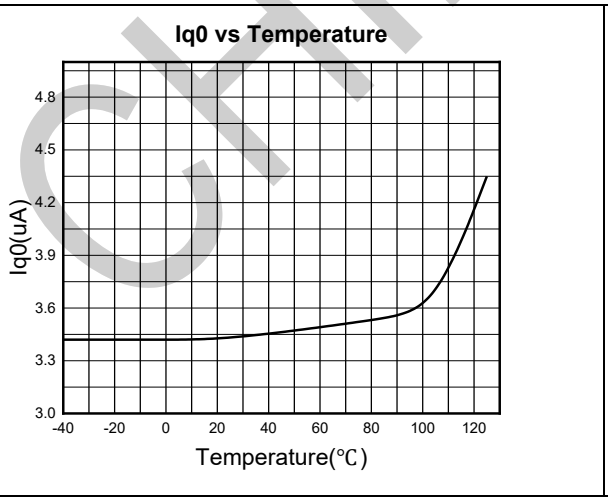
Test conditions: TA = 25°C, VDD = 12V, unless otherwise specified.

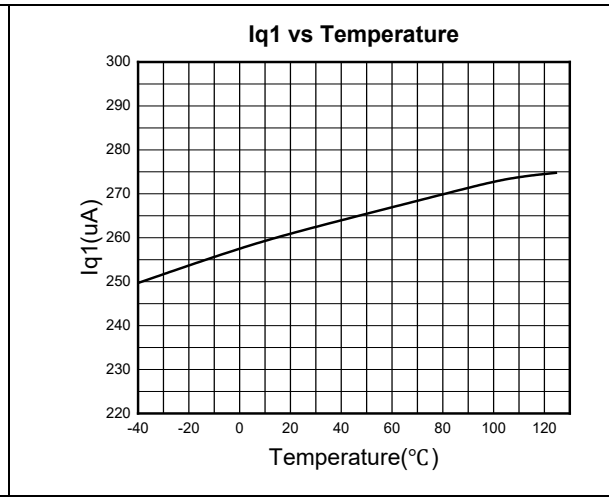
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply						
Standby Mode Supply Current	Iq0	INA=INB=0V		3.2	6.5	μA
Operating Supply Current	Iq1			235	410	μA
Output Enable Time	T1	VDD > VUVLO and INA or INB input high		10		us
Logic Level Input						
Input High Voltage	VIH		1.2			V
Input Low Voltage	VIL				0.4	V
Input Logic Hysteresis	$V_{IN\ HYS}$			0.15		V
Input High-Level Current	I_{INH}	INA or INB=5V		4.25		μA
Input Low-Level Current	I_{INL}	INA or INB=0V		0	1	μA
Input Pull-down Resistor	RIN		0.8	1.2	1.6	MΩ
Output						
HS On-Resistance	Rhs	ILOAD=300mA	0.2	0.45	0.9	Ω
LS On-Resistance	Rls	ILOAD=300mA	0.125	0.25	0.5	Ω
Body Diode Forward Voltage	V_D	IOUT=1A		0.8		V
Dead Time	Tdead			200		ns
ZCD shutdown time	T_ZCD	INA or INB from 10-00, time from OUTA、OUTB current less than ZCD current to output shutdown		1.6		ms
Protection Circuits						
VDD Undervoltage Reset Voltage	V_{UVLO_R}		3.6	4	4.4	V
VDD Undervoltage Lockout Voltage	V_{UVLO_F}		3.45	3.85	4.25	
VDD Undervoltage Protection Hysteresis	V_{UVLO_H}			0.15		V
Overcurrent Protection	OCP			3.5		A
Overcurrent Protection Filter Time	T_{OCP}			1.5		μs
Overcurrent Protection Retry Time	T_{RETRY}			1.6		ms
Thermal Shutdown Threshold	OTP			160		°C
Thermal Protection Hysteresis	T_{HYS}			30		°C



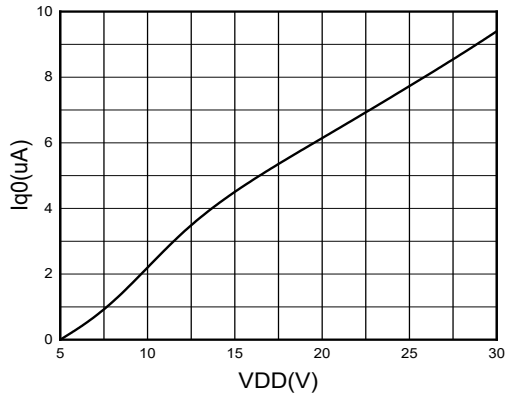
11.6 Characteristics Curve

Test conditions: TA = 25°C, VDD = 12V, unless otherwise specified.

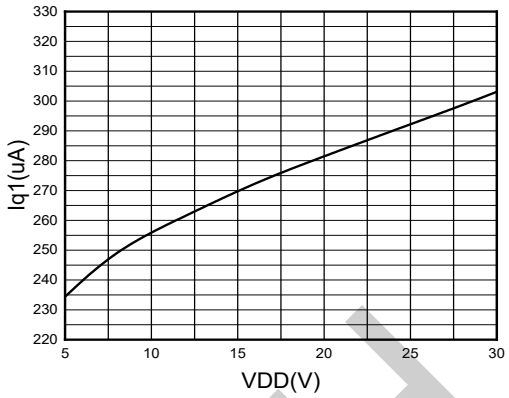




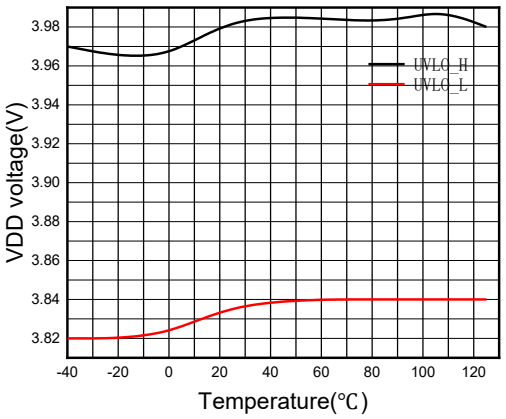
Iq0 vs VDD



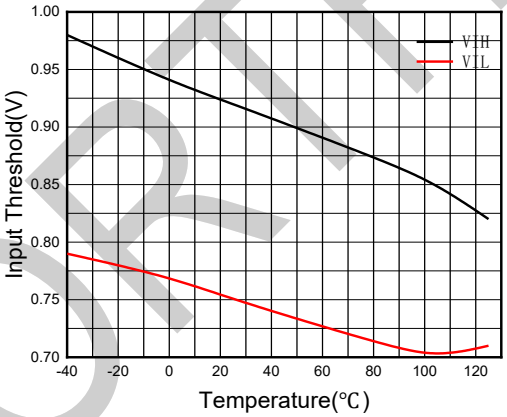
Iq1 vs VDD



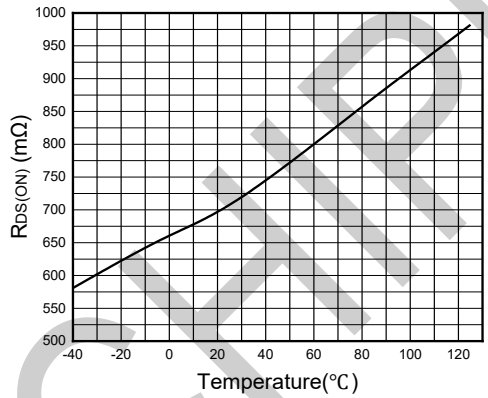
VDD UVLO vs Temperature



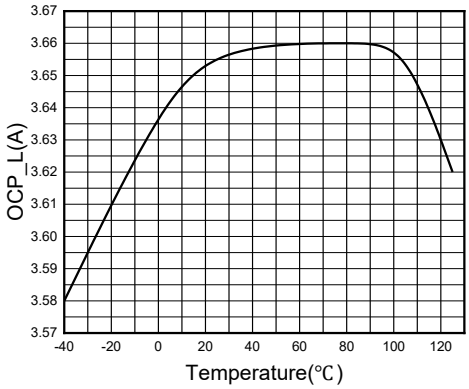
Input Threshold vs Temperature



HS+LS Rdson vs Temperature



OCP_L vs Temperature



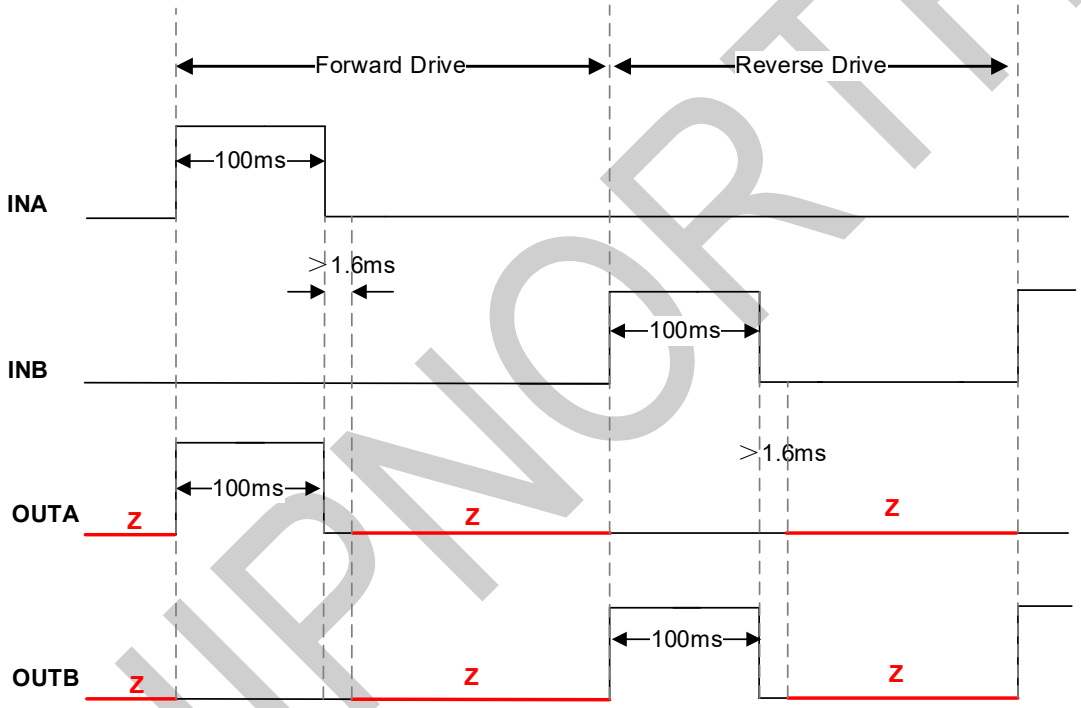
12 Detailed Description

12.1 Overview

CN8032 is a bi-direction relay driver circuit, used to control magnetic bi-direction relays. With high output current capability and ultra-low power consumption, it can be widely used in intelligent electro-meter and other related fields.CN8032 is available in SOT23-6 and SOP-8 package.

12.2 Back EMF Protection Function

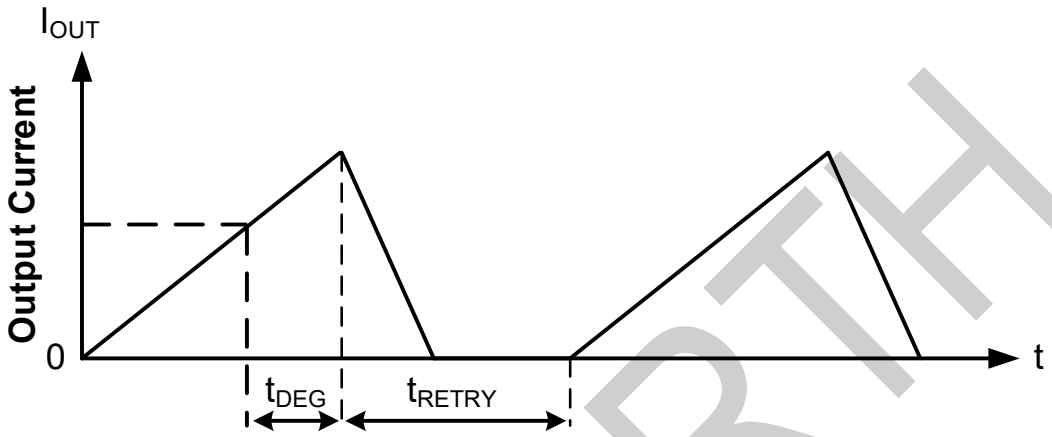
Description: To prevent potential destructive effects caused by back electromotive force (EMF), the CN8032 incorporates an anti-back EMF function. Through internal logic configuration, before the INA/INB inputs enter the "00" high-impedance off state, the internal logic control actually inserts an additional "11" state. This function allows the remaining inductive energy from the relay coil to be discharged to ground through the two NMOS transistors, effectively reducing chip damage due to back EMF.



Note: INA and INB are externally driven control logic, OUTA and OUTB are the output waveforms, and Z indicates that the output is in a high-impedance state.

12.3 Over Current Protection

Each FET is equipped with an analog current-limiting circuit that restricts the current flowing through the FET by eliminating the gate drive. If the analog current limit persists for longer than tDEG, all FET in the H-bridge will be disabled. Operation will automatically resume after tRETRY. Both the high-side and low-side FETs can detect overcurrent conditions. Shorting or grounding the OUTA pin to the OUTB pin will result in overcurrent.

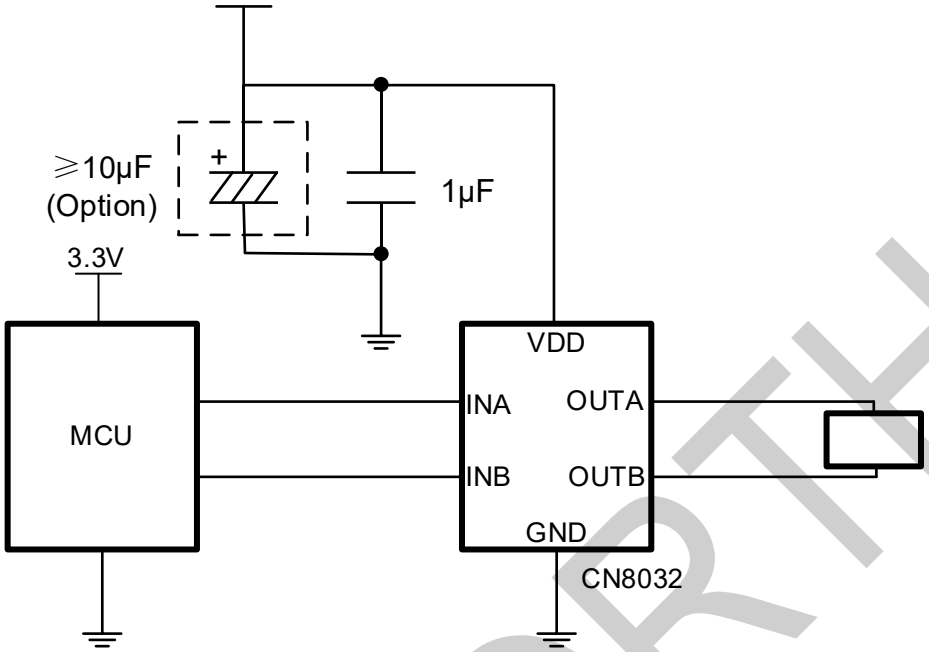


12.4 Thermal Shutdown

If the chip temperature exceeds 160°C, all FET in the H-bridge are disabled. Operation is automatically resumed when the chip temperature drops below 130°C.

13 Application information

13.1 Typical applications



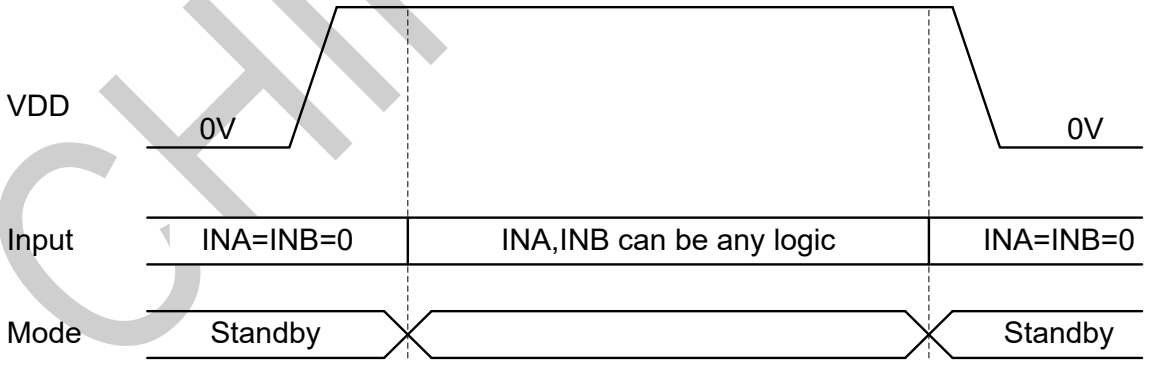
13.2 Design requirements

Design parameters	Symbol	Value
Relay Supply Voltage	VDD	12V
Logic High	IN	3.3V
Relay Current RMS	IOUT	1A

13.3 Design Procedure

13.3.1 VDD Power-Up

Make sure that the input signals INA and INB pins remain low during VDD power-up and power-down.



13.3.2 Low power operation

When INA and INB become low， OUTA and OUTB are grounded, When the current of OUTA and OUTB is less than 1.6ms of current compared to ZCD, OUTA and OUTB enter a high-impedance state and the chip enters sleep mode to minimize system power consumption.

13.3.3 Input Capacitance

Proper input capacitance is an important factor in the design of a relay drive system. In general, the larger the capacitance, the better, with the disadvantage of increased cost and physical size.

The size of the required input capacitance depends on a number of factors including.

- Maximum current required by the relay system.
- Power supply capacitance and current source capability.
- Parasitic inductance between the power supply and relay system.

The inductance between the power supply and the relay drive system limits the rate of change of the power supply current. If the input capacitor capacity is too small, the system responds to excessive current demand or Relay dumps with voltage changes. If a large enough input capacitor is used, the Relay voltage will remain stable and large currents will be available quickly.

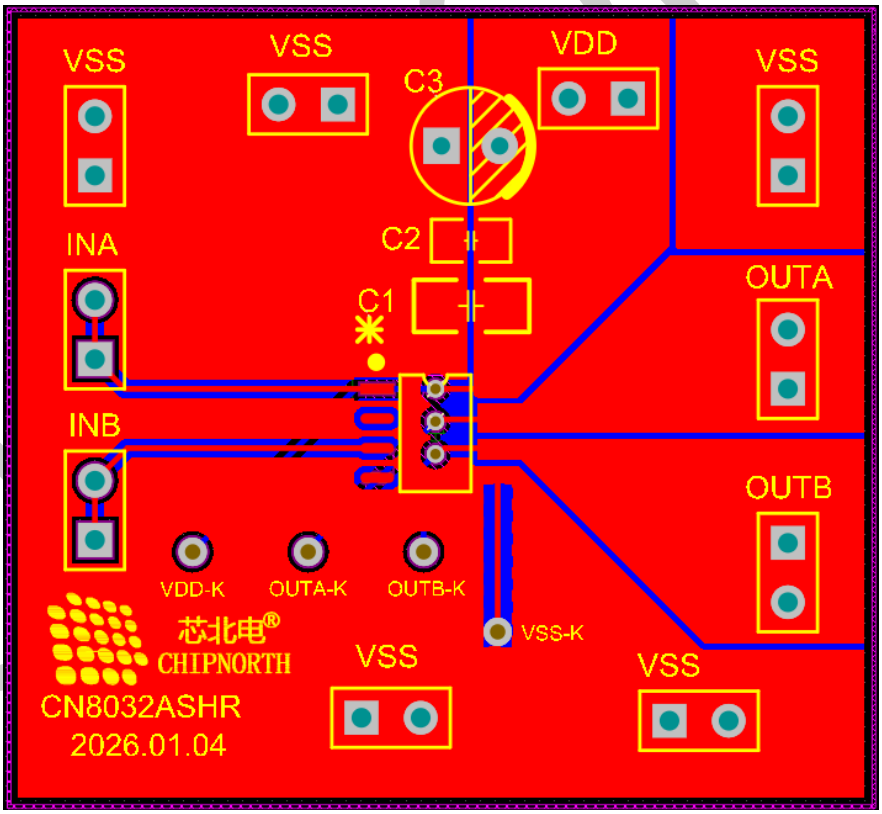
Datasheets usually provide recommended values, but system-level testing is required to determine the proper capacitance.

13.4 PCB Layout Guidelines

13.4.1 PCB Layout Recommendations

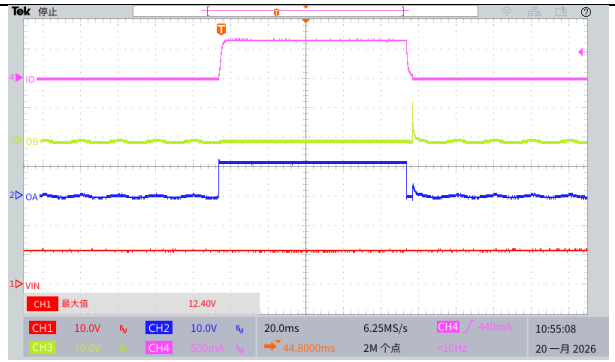
- It is recommended that low ESR ceramic capacitors be used to connect the VDD pin to GND, with a recommended rating of 1 μF. These capacitors should be placed as close as possible to the VDD pin, and the alignment should be as coarse as possible to connect to the ground plane.

13.4.2 PCB Layout

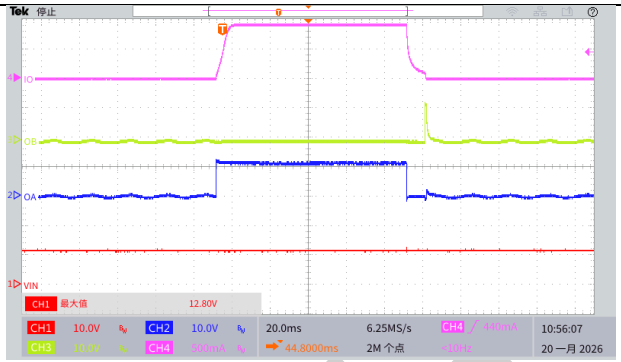


13.5 Operating waveforms

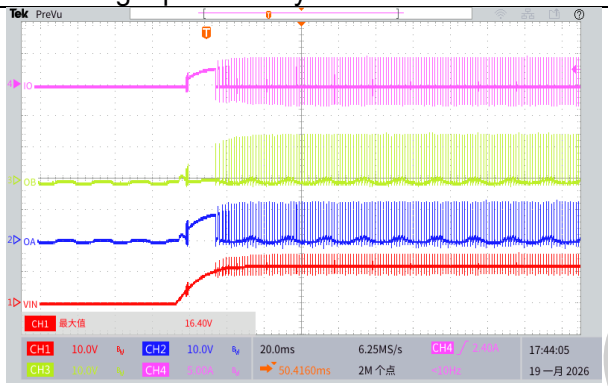
Test conditions: TA = 25°C, VDD = 12V, unless otherwise specified.



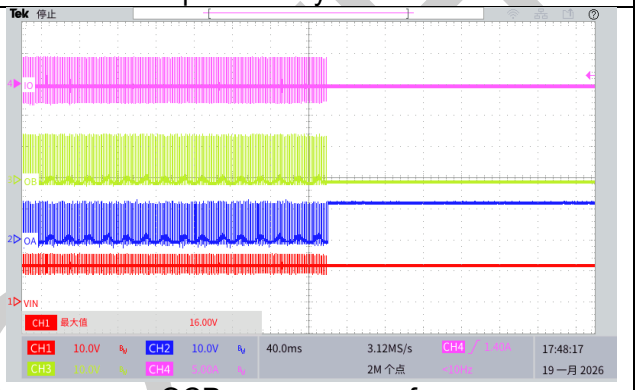
Single-phase relay drives waveforms



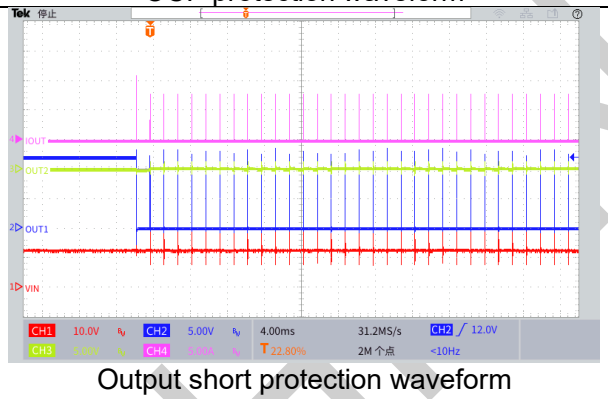
Three-phase relay drive waveform



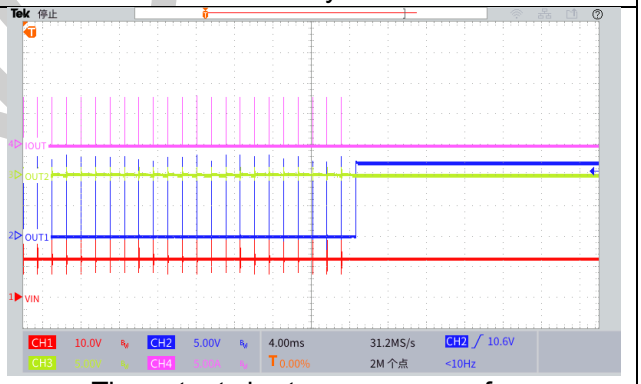
OCP protection waveform



OCP recovery waveform



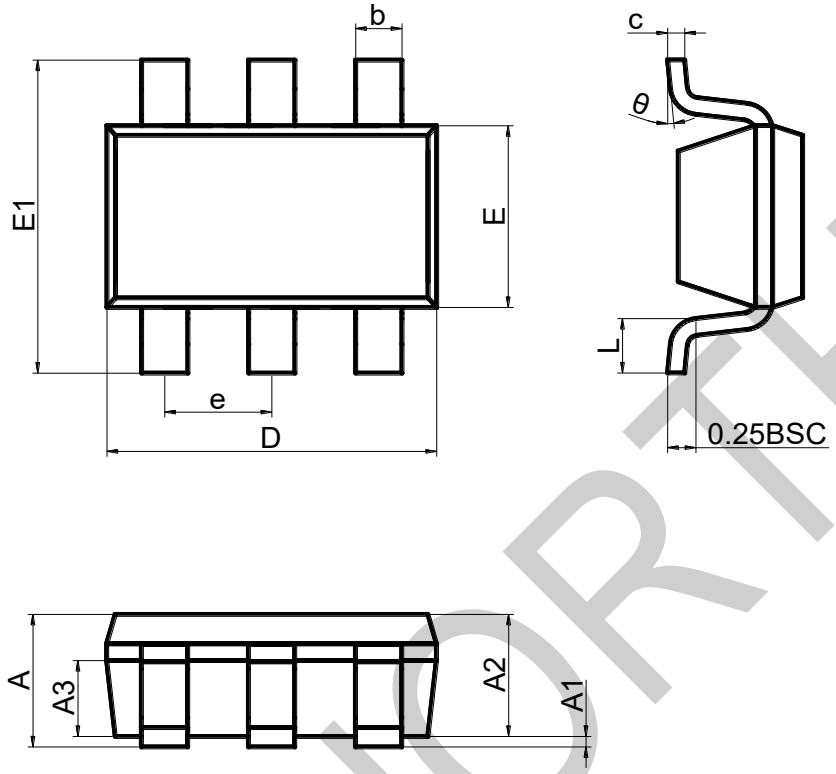
Output short protection waveform



The output short recovery waveform

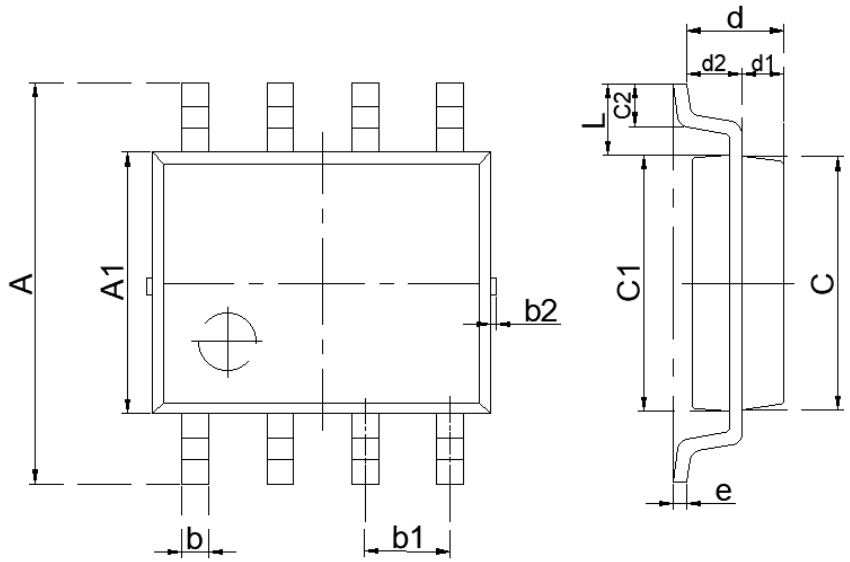
14 Package Information

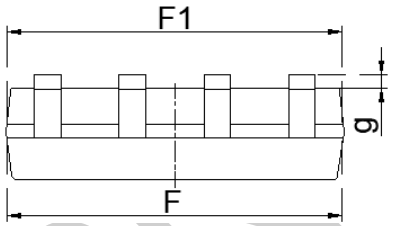
SOT23-6



Dimension / Symbol	Min （mm）	Nom (mm)	Max (mm)
A	1.05	1.15	1.25
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.10	0.152	0.20
D	2.82	2.92	3.02
E	1.51	1.61	1.7
E1	2.65	2.80	2.95
e	-	0.95	-
L	0.30	0.42	0.57

SOP-8





Symbol \ Value	Min（mm）	Max（mm）
A	5.8	6.2
A1	3.8	4.0
b	0.38	0.50
b1	1.17	1.37
b2	0	0.15
C	3.75	3.95
C1	3.8	4.0
C2	0.5	0.7
d	1.35	1.45
d1	0.55	0.65
d2	0.75	0.85
e	0.18	0.25
L	0.9	1.2
F	4.75	4.95
F1	4.8	5.0
g	0.06	0.16

15 Important Statement

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16 Revision History

Date	Version Number	Revision Notes
2026/05/20	R1.0	Official Release
2026/05/28	R1.1	Update package dimensions
2026/06/03	R1.2	Update marking information
2026/06/18	R1.3	Update recommended operating conditions