6 V to 40 V, Power Line Carrier Driver

1 Description

The CN6222 is a line driver designed for power line communication (PLC) applications, suitable for driving lines in broadband power line communication (PLC) systems. The chip incorporates two current-feedback amplifiers with extremely low distortion, ensuring that out-of-band signals transmitted within the power line communication (PLC) frequency range comply with specifications. The chip can handle significant variations in power line communication (PLC) channel impedance and maintains signal transmission quality even under heavy loads.

The chip can operate at 75% or 90% of the set static current via a digital control port. This can be adjusted via software based on channel conditions, further optimizing the chip's drive performance.

The chip's operating voltage range extends up to 40V. Integrated protection modules, including over current and over temperature protection, ensure stable and reliable performance under various conditions, delivering superior performance in PLC applications.

The CN6222 is available in a QFN 5x4 - 24-pin package.

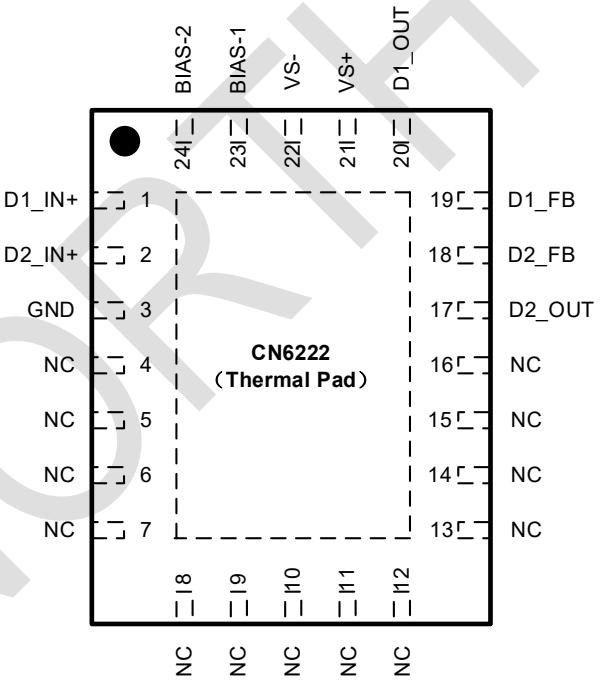
2 Features

- Operating voltage: 6V to 40V
- Wide band signal bandwidth: 80MHz
- Output swing: 16Vpp at 50Ω load, Vs+=12V
- Third-harmonic suppression:
  -72dBc @ 10MHz / 2Vpp / 50Ω load
  -78dBc @ 1MHz / 2Vpp / 50Ω load
- Second-harmonic suppression:
  -64dBc @ 10MHz / 2Vpp / 50Ω load
  -57dBc @ 1MHz / 2Vpp / 50Ω load
- Operating current is externally set and can be digitally controlled
- Slew rate: 1440 V/μs
- TTL/CMOS compatible
- Temperature range: -40°C to +85°C

3 Applications

- Power Line Communication

4 Pinout



5 Ordering information

Product Number	Package	Quantity/Tape
CN6222QLR	QFN5X4-24L	5000/Tape

6 Marking

Product Number	Marking
CN6222QLR	CN6222 YYWW

Note: YY=Year WW=Week.

Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level (MSL):3

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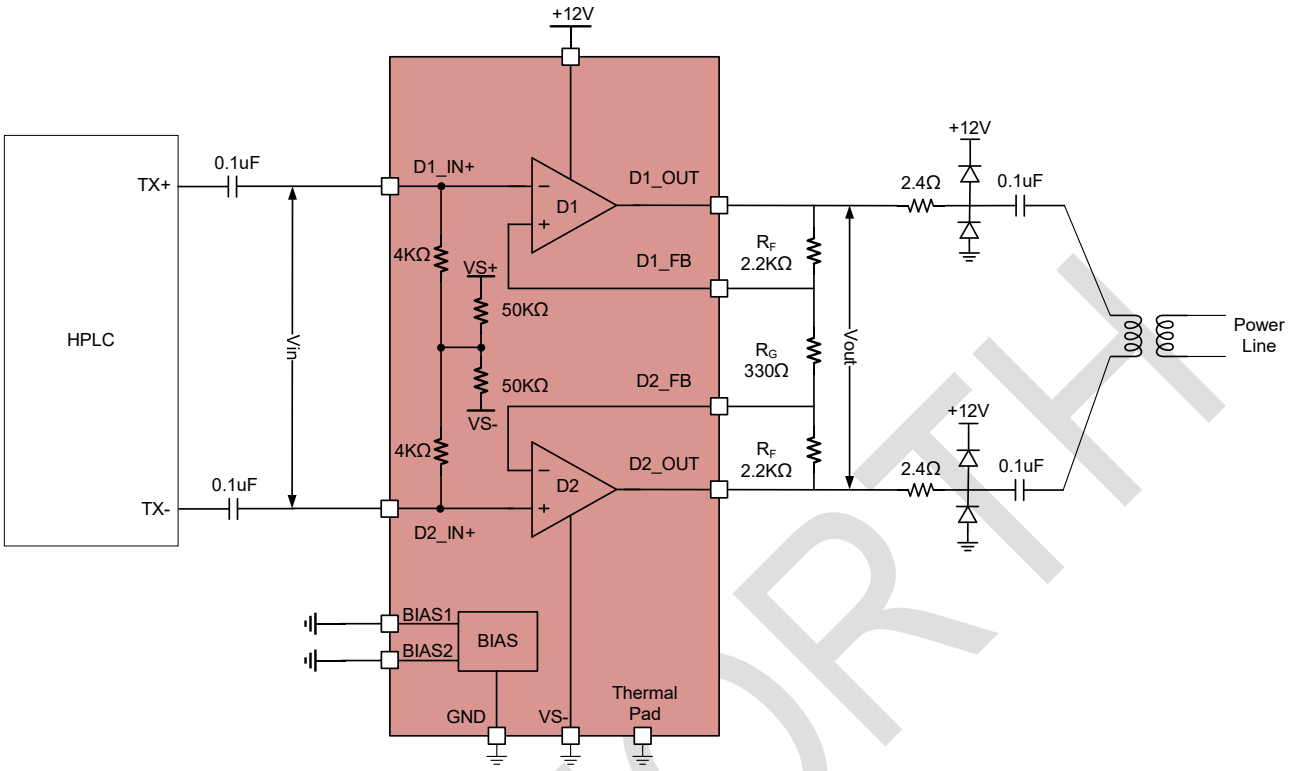
7 Typical Application



$$A_V = \frac{R_F}{R_G} \times 2 + 1$$

8 Pin Descriptions

Pin No.	Pin Name	Descriptions
1	D1_IN+	OP1 In-phase input
2	D2_IN+	OP2 In-phase input
3	GND	GND
4~16	NC	NC
17	D2_OUT	OP2 Output
18	D2_FB	OP2 Inverting input
19	D1_FB	OP1 Inverting input
20	D1_OUT	OP1 Output
21	VS+	Positive supply terminal
22	VS-	Negative supply terminal
23	BIAS-1	Enable pin1
24	BIAS-2	Enable pin2
25	EP (1)	Heat sink base, grounded

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9 Specifications

9.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
VS+	VS+ Maximum voltage	44	V
VBIAS	Logic pins BIAS1/BIAS2 input range	-0.3~44	V
T_J	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55~150	°C

Note1: Stress exceeds these ratings listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability.

9.2 ESD Ratings

Discharge mode	Standard	Value	Units
HBM	ESDA/JEDEC JS-001-2017	±2000	V
CDM	ANSI/ESDA/JEDEC JS-002-2022	±2000	V

9.3 Thermal Information

Symbol	Parameter	Value	Unit
θJA	Junction to ambient	40	°C/W
θJC(top)	Junction to case（top）	35	°C/W
θJB	Junction to case（bottom）	21	°C/W

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10 Electrical Characteristics

(Vs+=12V，T_A=25°C，A_V=14.3V/V，The differential load resistor RL is connected directly to the output via a 0.1 μF capacitor, unless otherwise specified.)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{DD}		6	12	40	V
Shutdown Current	I_{DD1}	BIAS-1 = BIAS-2 = 5V		330	500	μA
Quiescent Current	I_{DD2}	BIAS-1 = BIAS-2 = 0V		32	40	mA
	I_{DD3}	BIAS-1 = 5V，BIAS-2 = 0V		29	38	mA
	I_{DD4}	BIAS-1 = 0V，BIAS-2 = 5V		24	32	mA
Input Voltage Range	V_{IN}			1	3	Vpp
Input High Voltage	V_{IH}		1.9			V
Input Low Voltage	V_{IL}				0.8	V
Small signal bandwidth	SSBW	Vo=2Vpp，R_L = 50Ω，Full Bias		81		MHz
		Vo=2Vpp，R_L = 50Ω，Low Bias		78		MHz
Large signal bandwidth	LSBW	Vo=10Vpp，R_L = 50Ω，Full Bias		80		MHz
		Vo=10Vpp，R_L = 50Ω，Low Bias		77		MHz
Swing rate	SR	Vo=16Vpp（10%-90%）		1440		V/us
Second-harmonic distortion	HD2	Fc = 1MHz, V_{OUT} = 2Vpp-diff, R_L = 50Ω		-57		dBc
		Fc = 10MHz, V_{OUT} = 2Vpp-diff, R_L = 50Ω		-64		dBc
Third-harmonic distortion	HD3	Fc = 1MHz, V_{OUT} = 2Vpp-diff, R_L = 50Ω		-78		dBc
		Fc = 10MHz, V_{OUT} = 2Vpp-diff, R_L = 50Ω		-72		dBc
Differential output slew rate	VODiff	VS=+12V, RL_Diff=50Ω		16		Vpp
		VS=+12V, RL_Diff=20Ω		13		Vpp

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11 Operating Waveform

(T_A=25°C，Vs+=12V，IN1-IN2=1Vpp，RF=2.2kΩ，RG=330Ω，AV=14.3V/V.)

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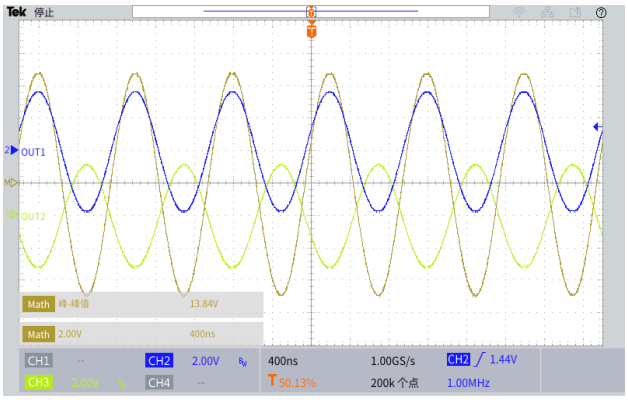
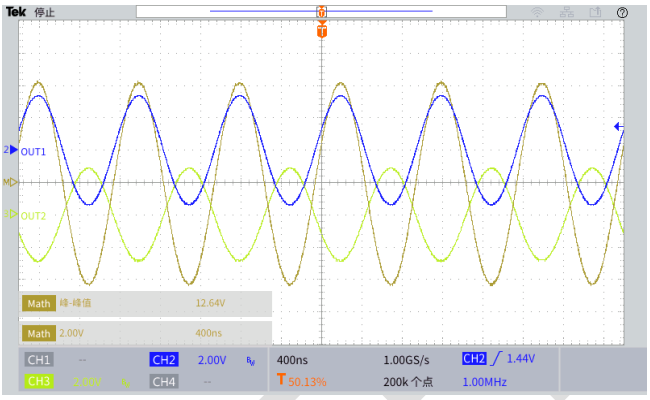
<td> 

f=1MHz、No load</td>
<td> 

f=1MHz、RL_Diff=50Ω</td>
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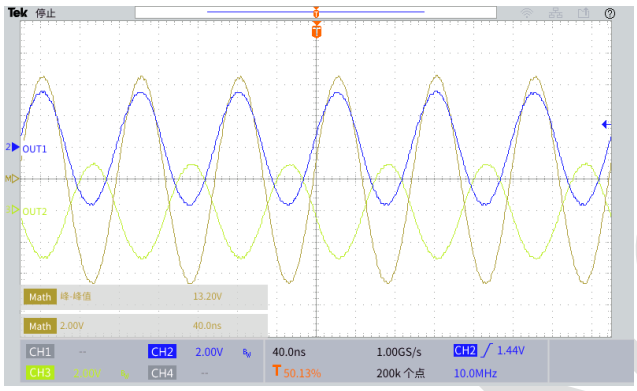
<td> 

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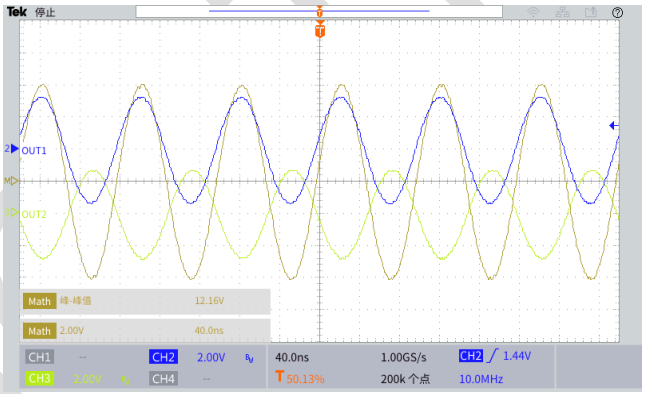
<td> 

f=10MHz、RL_Diff=50Ω</td>
</tr>
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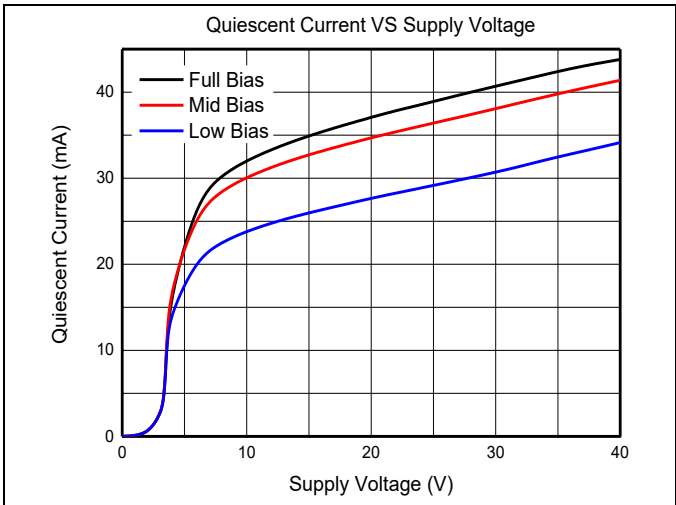
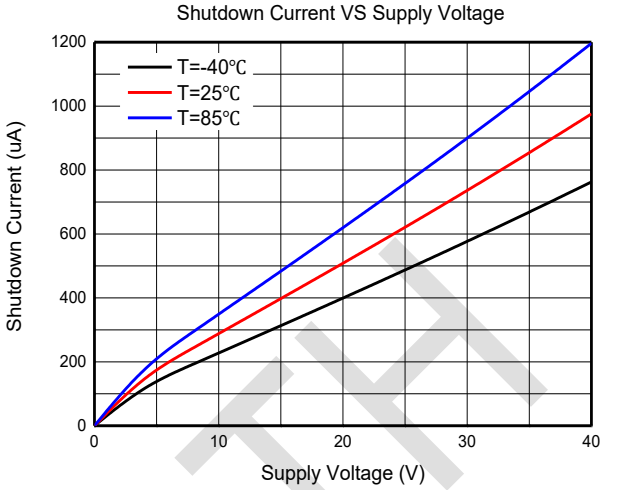
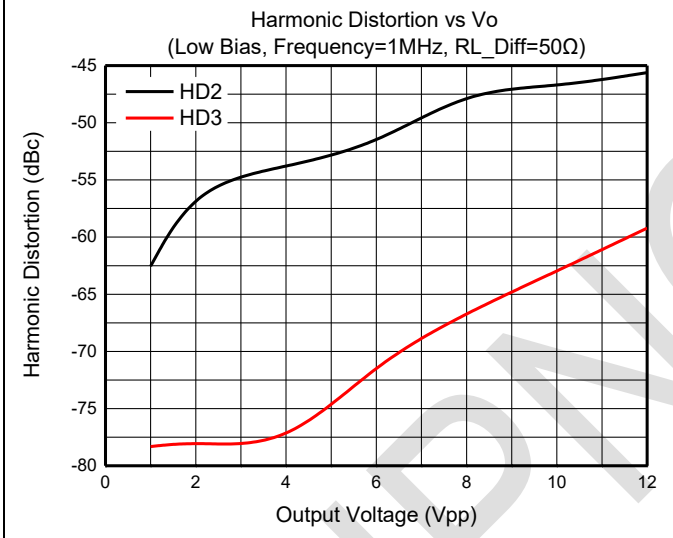
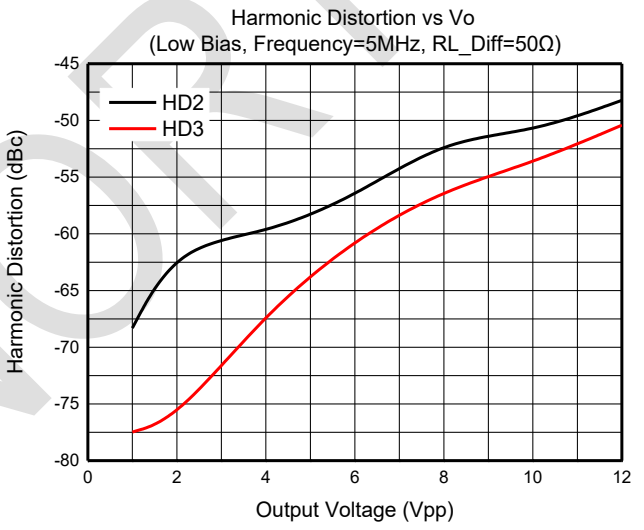
12 Performance Curve

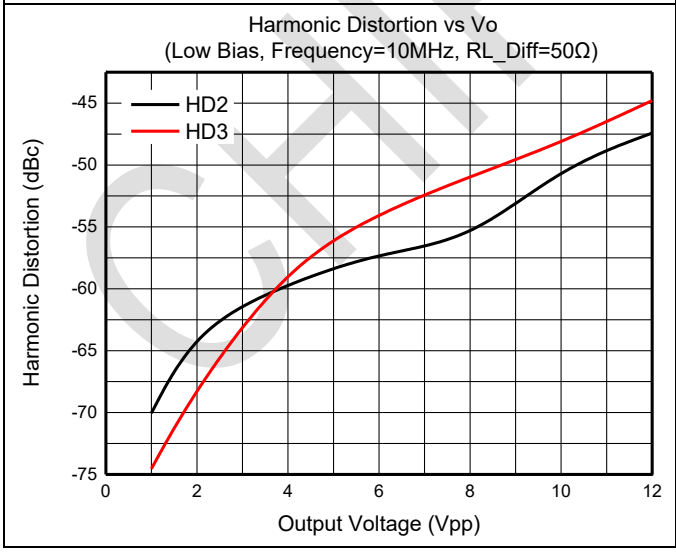
(T_A=25°C，Vs+=12V，RF=2.2kΩ，RG=330Ω，AV=14.3V/V.)

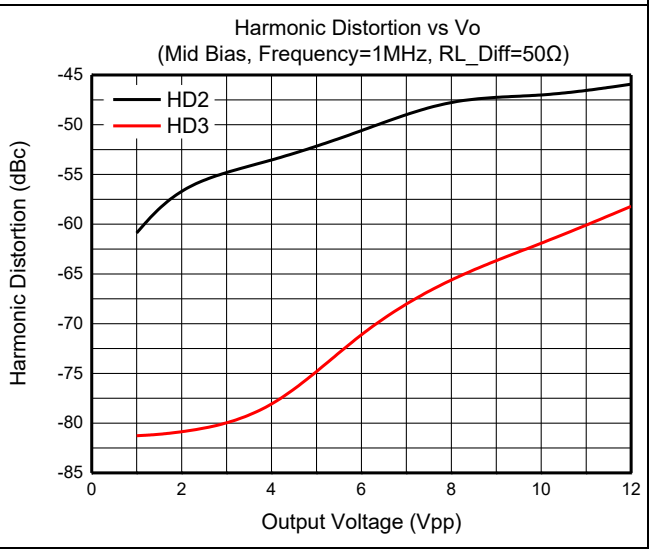












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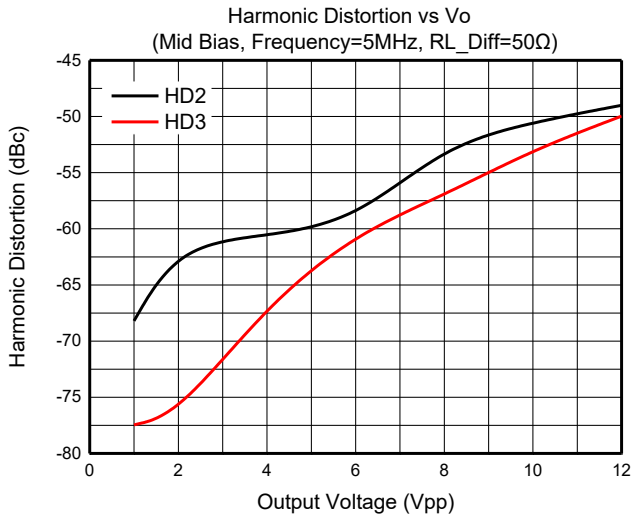
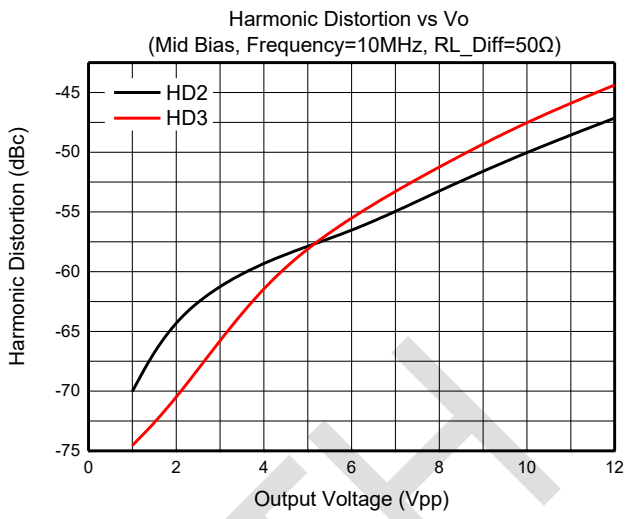
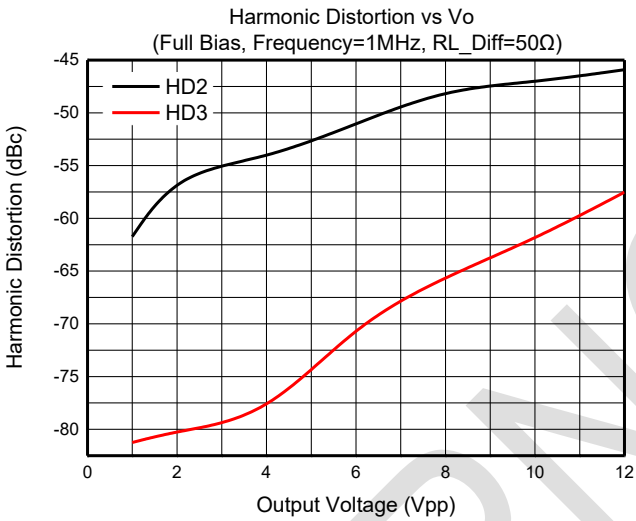
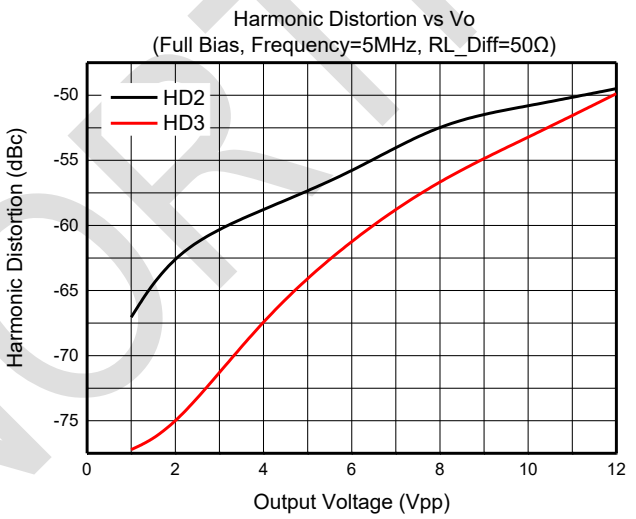
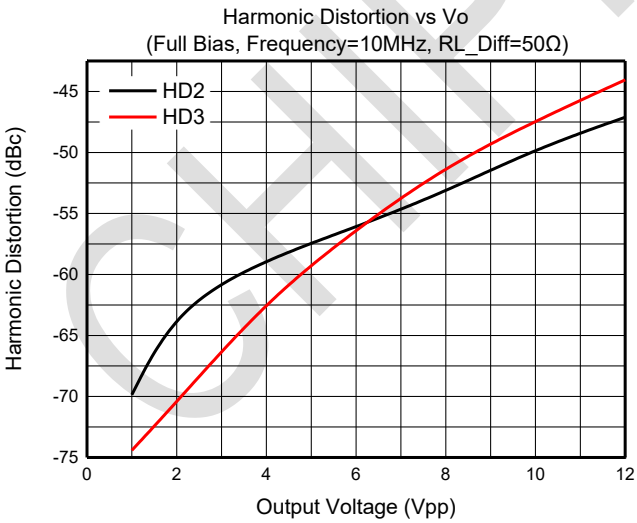
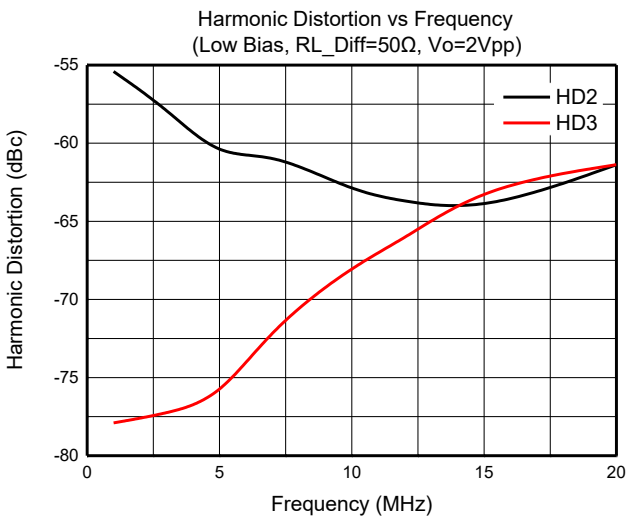

Harmonic Distortion vs Vo
(Mid Bias, Frequency=5MHz, RL_Diff=50Ω)
HD2
HD3
Harmonic Distortion (dBc)
Output Voltage (Vpp)


Harmonic Distortion vs Vo
(Mid Bias, Frequency=10MHz, RL_Diff=50Ω)
HD2
HD3
Harmonic Distortion (dBc)
Output Voltage (Vpp)


Harmonic Distortion vs Vo
(Full Bias, Frequency=1MHz, RL_Diff=50Ω)
HD2
HD3
Harmonic Distortion (dBc)
Output Voltage (Vpp)


Harmonic Distortion vs Vo
(Full Bias, Frequency=5MHz, RL_Diff=50Ω)
HD2
HD3
Harmonic Distortion (dBc)
Output Voltage (Vpp)


Harmonic Distortion vs Vo
(Full Bias, Frequency=10MHz, RL_Diff=50Ω)
HD2
HD3
Harmonic Distortion (dBc)
Output Voltage (Vpp)


Harmonic Distortion vs Frequency
(Low Bias, RL_Diff=50Ω, Vo=2Vpp)
HD2
HD3
Harmonic Distortion (dBc)
Frequency (MHz)

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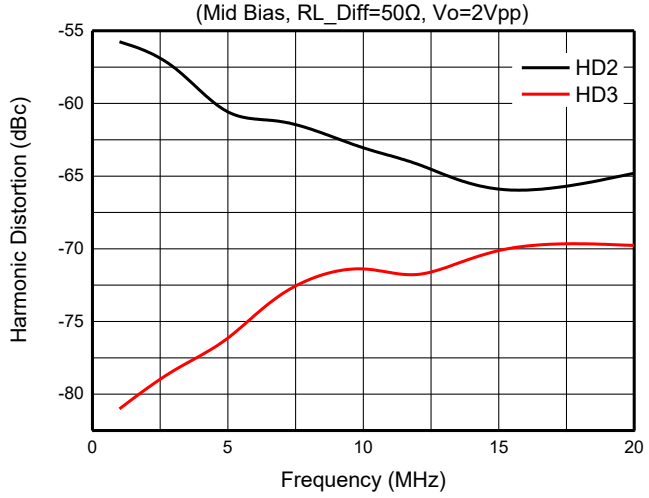
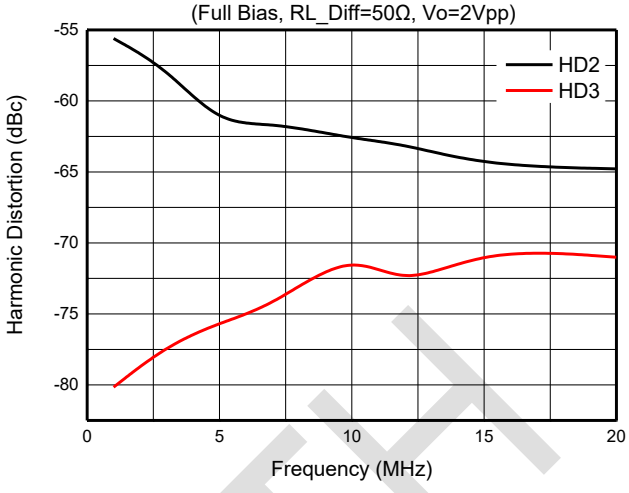
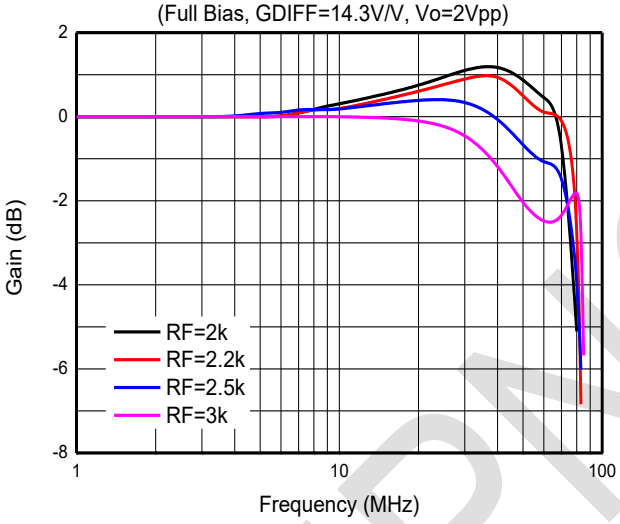
Harmonic Distortion vs Frequency
(Mid Bias, RL_Diff=50Ω, Vo=2Vpp)



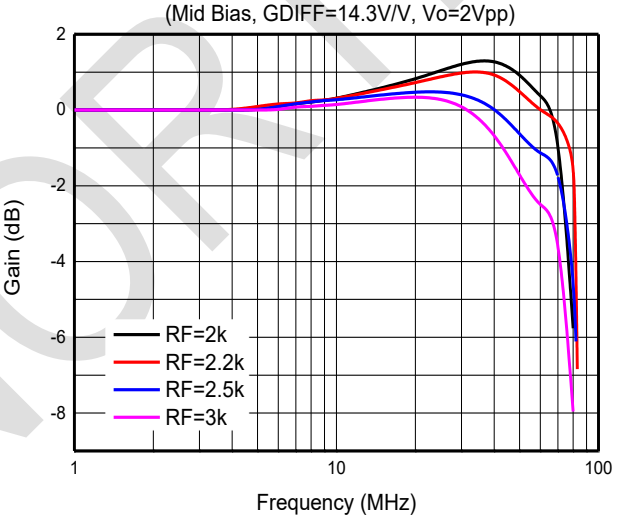
Harmonic Distortion vs Frequency
(Full Bias, RL_Diff=50Ω, Vo=2Vpp)



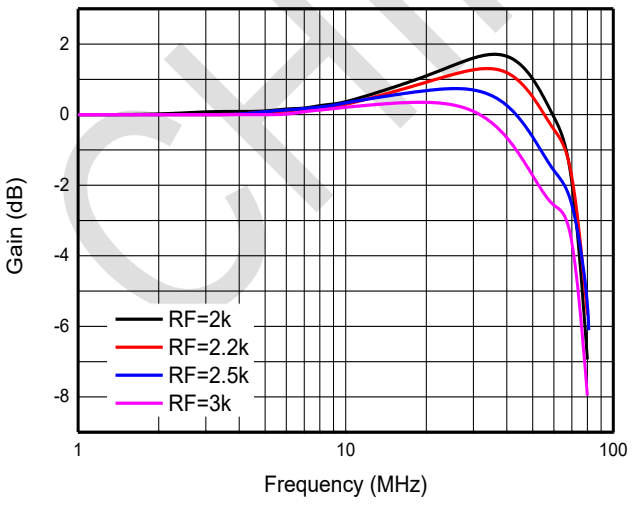
Small-Signal Frequency Response vs RF
(Full Bias, GDIFF=14.3V/V, Vo=2Vpp)



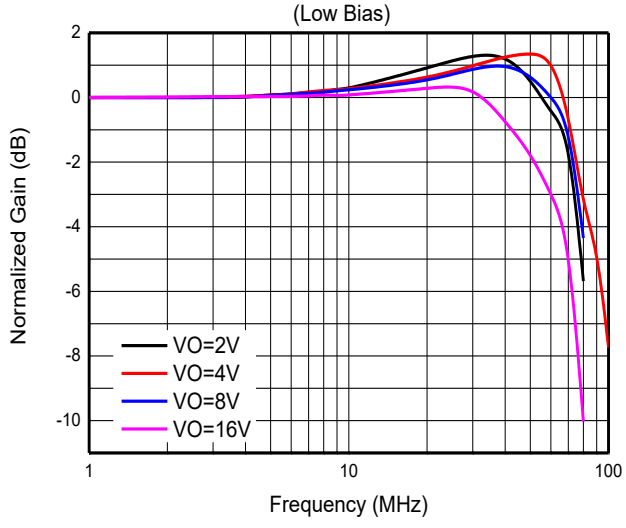
Small-Signal Frequency Response vs RF
(Mid Bias, GDIFF=14.3V/V, Vo=2Vpp)



Small-Signal Frequency Response vs RF
(Low Bias, GDIFF=14.3V/V, Vo=2Vpp)



Large Signal Frequency Response vs Vo
(Low Bias)



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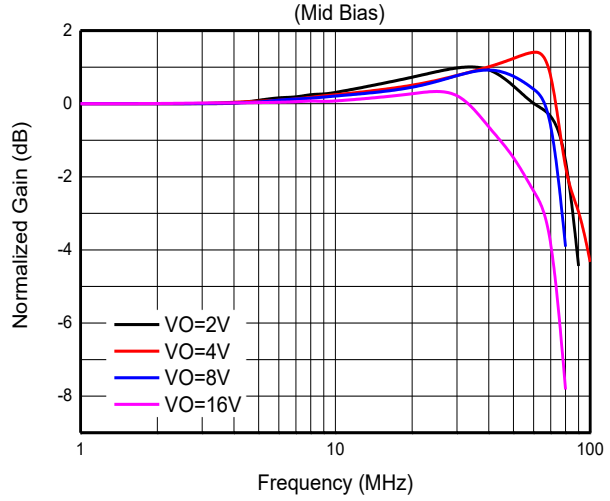
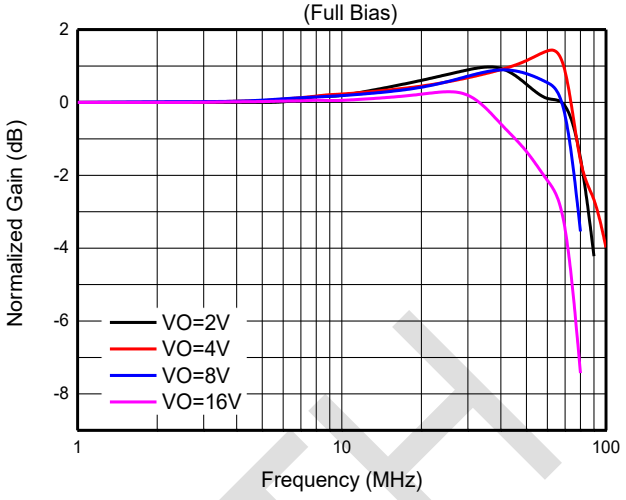
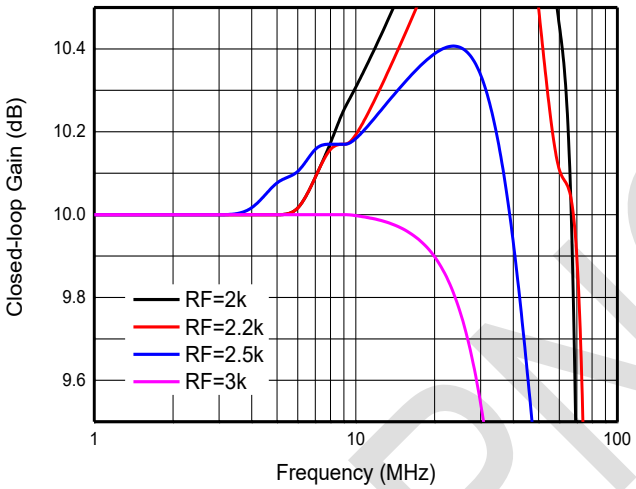
Large Signal Frequency Response vs Vo
(Mid Bias)



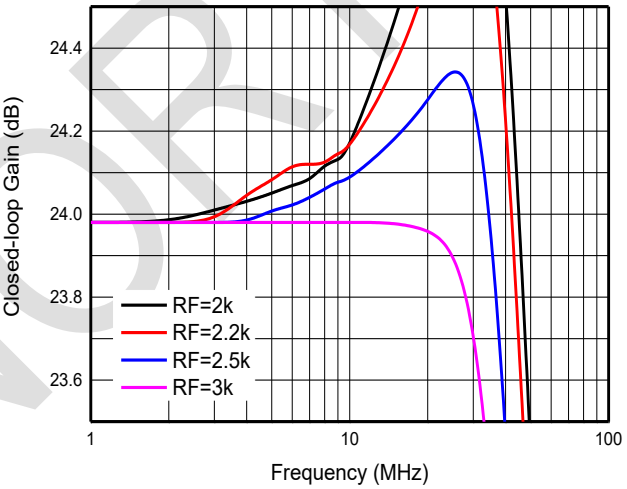
Large Signal Frequency Response vs Vo
(Full Bias)



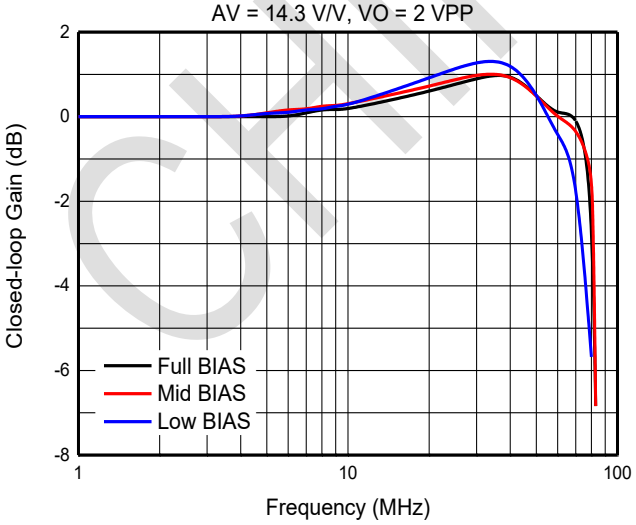
Small-Signal Gain Flatness vs RF
AV = 14.3 V/V, VO = 2 VPP



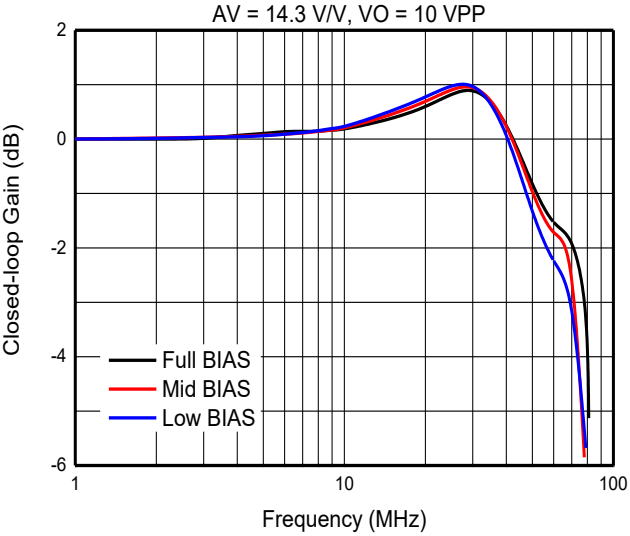
Large-Signal Gain Flatness vs RF
AV = 14.3 V/V, VO = 10 VPP



Small-Signal Frequency Response vs Bias Modes
AV = 14.3 V/V, VO = 2 VPP



Large-Signal Frequency Response vs Bias Modes
AV = 14.3 V/V, VO = 10 VPP



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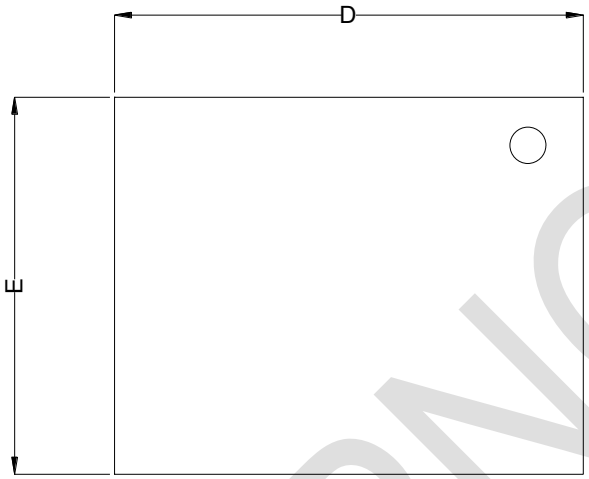
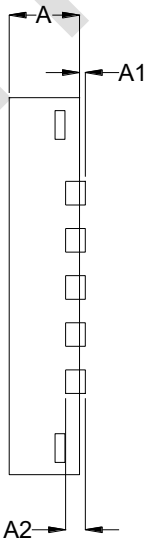
13 Package Information

QFN 5X4 - 24L

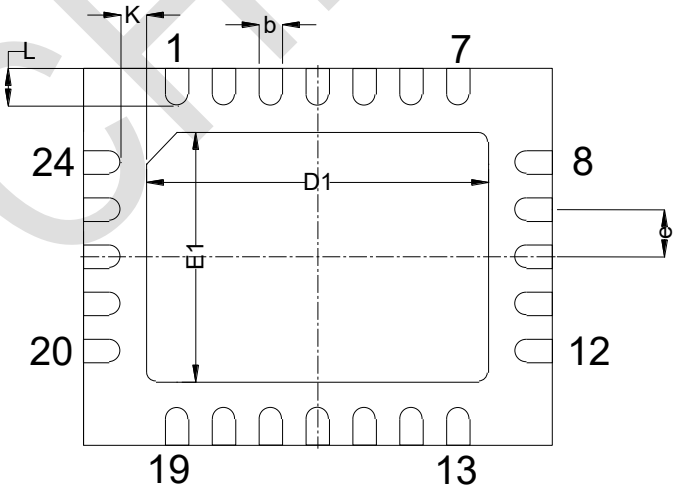
Size(mm) / Symbol	Min.	Typ.	Max.	Size(mm) / Symbol	Min.	Typ.	Max.
A	0.7	0.75	0.8	D1	3.55	3.65	3.75
A1	0.00	-	0.05	E1	2.55	2.65	2.75
A2	0.203REF			e	0.50TYP		
b	0.225	0.250	0.275	K	0.275TYP		
D	4.90	5.00	5.10	L	0.30	0.40	0.50
E	3.90	4.00	4.10				



Top View



Side View



Bottom View

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14 Important Statement

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