芯北电®
CHIPNORTH

CN3501TER

5V/1W~2W Micropower Isolated Power Supply Special Chip

1 Description

The CN3501TER is a push-pull transformer driver specially designed for small size, low standby power consumption micropower isolated power supply, which can realize 5V-5V, 12V-5V isolated power supply with output power of 1~2W by matching the simple input/output filter capacitors, isolation transformer and rectifier circuits peripherally. The CN3501TER chip has an integrated oscillator to provide a pair of high-precision complementary signals to drive two N-channel MOSFET, which is designed according to the symmetrical structure of the chip to ensure the high symmetry of the two power MOSFET and avoid the bias magnetization of the circuit in the process of operation. A high-precision deadband control circuit is designed inside the chip to ensure that no commutation occurs under various operating conditions.

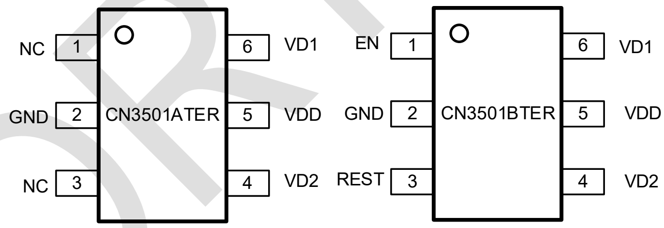
2 Features

- Push-pull topology
- Highly integrated, simple peripheral
- Built-in 24V/0.3Ω LDMOS
- 0.8A current clamp limiting, low short-circuit power consumption while improving capacitive load capability.
- 2.8-9V input voltage range
- External enable control for low standby power consumption and sleep function
- Adjustable switching frequency: 200K-1.8M with optional small transformer size.
- Continuous short-circuit protection, over-temperature protection, under-voltage protection, self-recovery
- Ambient temperature： -40°C ~ +105°C

3 Applications

- CAN, RS-485, RS-232, SPI, I2C, etc. Low-power Isolated Power Supplies
- Process Control
- Precision instruments\Medical instruments
- Distributed power supply, radio power supply, telecom power supply
- Low Noise Isolated USB Power Supplies
- Low noise filament power supply

4 Pinout



5 Ordering information

Product Number	Package	Quantity/Tape
CN3501ATER	SOT23-6	3000/Tape
CN3501BTER	SOT23-6	3000/Tape

6 Marking

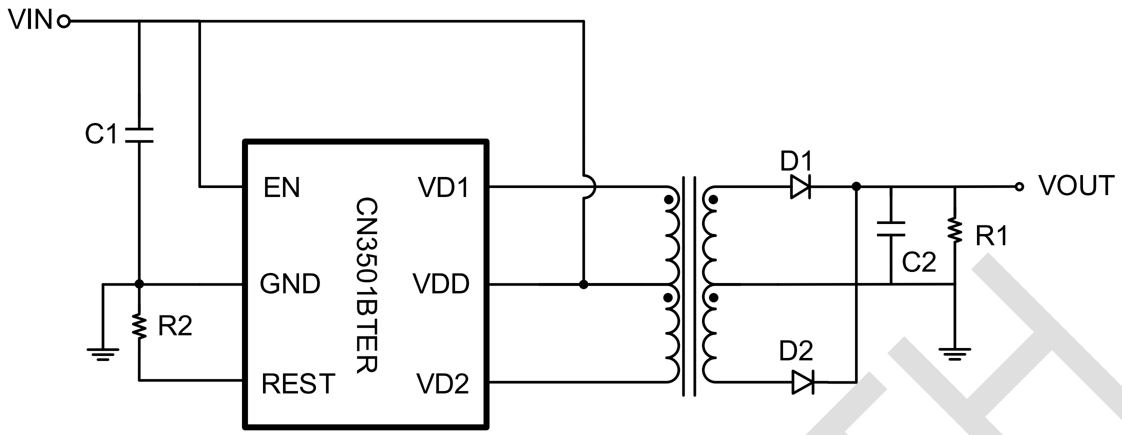
Product Number	Marking
CN3501ATER	3501A YYWW
CN3501BTER	3501B YYWW

Note: YY=Year WW=Week.

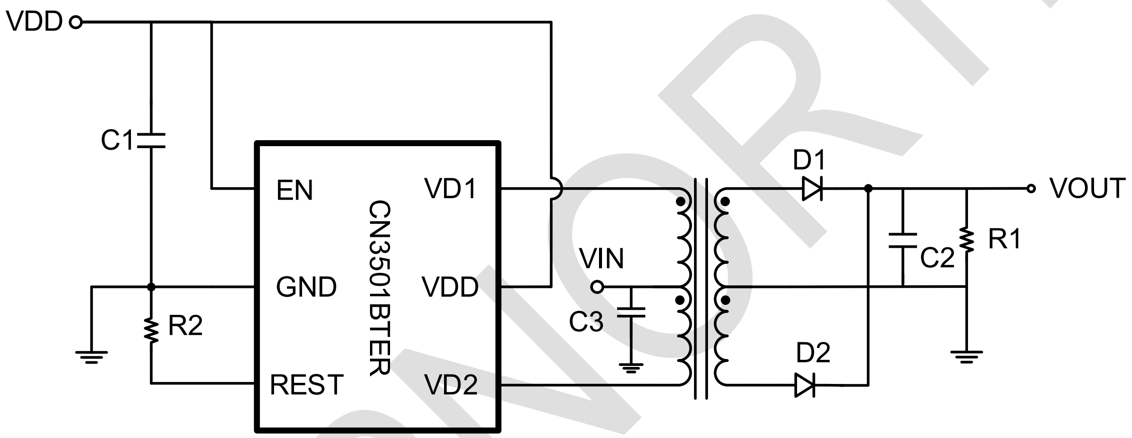
Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

7 Typical Application

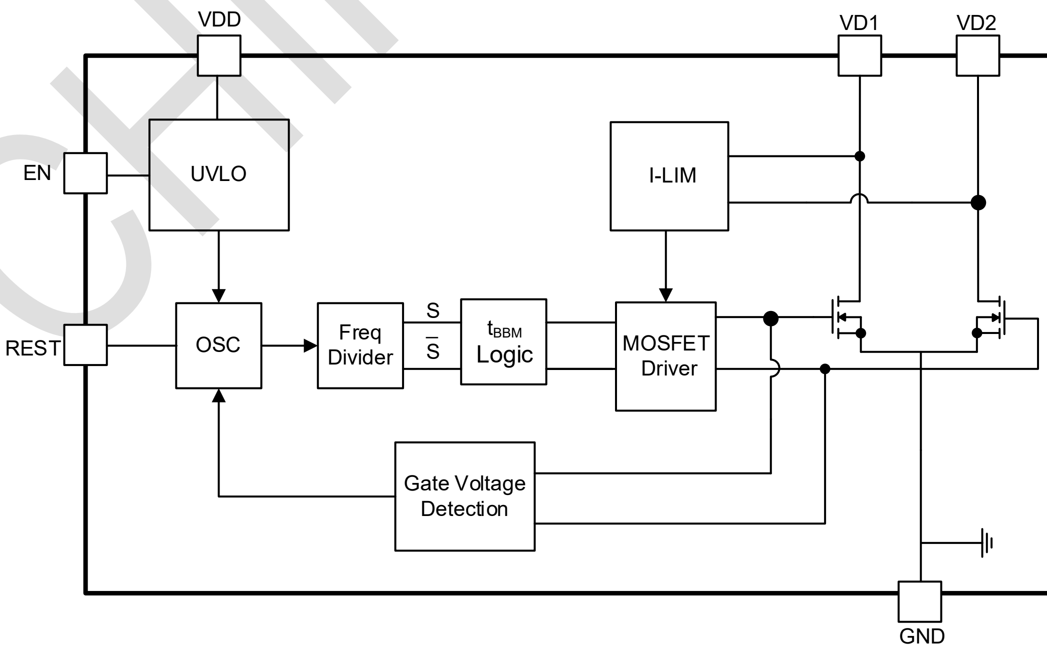


5V-5V Typical Application Circuit Diagram



12V-5V Typical Application Circuit Diagram

8 Block Diagram



9 Pin Descriptions

Pin No.		Pin Name	Description
CN3501A	CN3501B		
1、3	/	NC	No Connection
/	1	EN	Enable pin, high level active, drive the pin to high level can enable the chip, low level disable the chip, self-start can be connected EN to VIN
2	2	GND	GND
/	3	REST	This pin can be connected resistor to ground to set 200K-1.8M switching frequency, if the pin is shorted or floating, the switching frequency defaults to 360K.
4	4	VD1	Transformer drive output 1
5	5	VDD	power input, place a 10uF capacitor between VDD-GND and as close to the chip as possible
6	6	VD2	Transformer drive output 2

10 Specifications

10.1 Absolute Maximum Ratings

Parameter	Value	Units
Supply Input Voltage	10	V
EN Voltage	10	V
LDMOS Tube Drain Voltage	-0.3 ~ 24	V
LDMOS Tube Peak Current	0.8	A
Ambient Temperature	-40 ~105	°C
Soldering Temperature	260（soldering,10s）	°C
Storage Temperature Range	-55 ~ 150	°C

Note1: Stress exceeds these ratings listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability.

10.2 ESD Ratings

Discharge mode	Standardize	Value	Units
HBM	JEDECJS-001-2023	±2000	V
CDM	JEDECJS-002-2022	±2000	V
Latch up	JESD78F.02-2023	±800	mA

10.3 Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units
Operating Supply Voltage	V_{DD}	2.8	9	V
Input Capacitance Range	C_{IN}	4.7	10	μF
Output Capacitance Range	C_{OUT}	4.7		μF
LDMOS MOSFET drain current	I_{VD1}，I_{VD2}	0.5		A
Ambient Temperature	T_A	-40	105	°C

10.4 Thermal Information

Parameter	Package	Value	Unit
Junction to ambient($R\theta_{JA}$)	SOT23-6	137.7	°C/W
Junction to case($R\theta_{JC(top)}$)		57	°C/W
Junction to caseθjc（bot）		46	°C/W

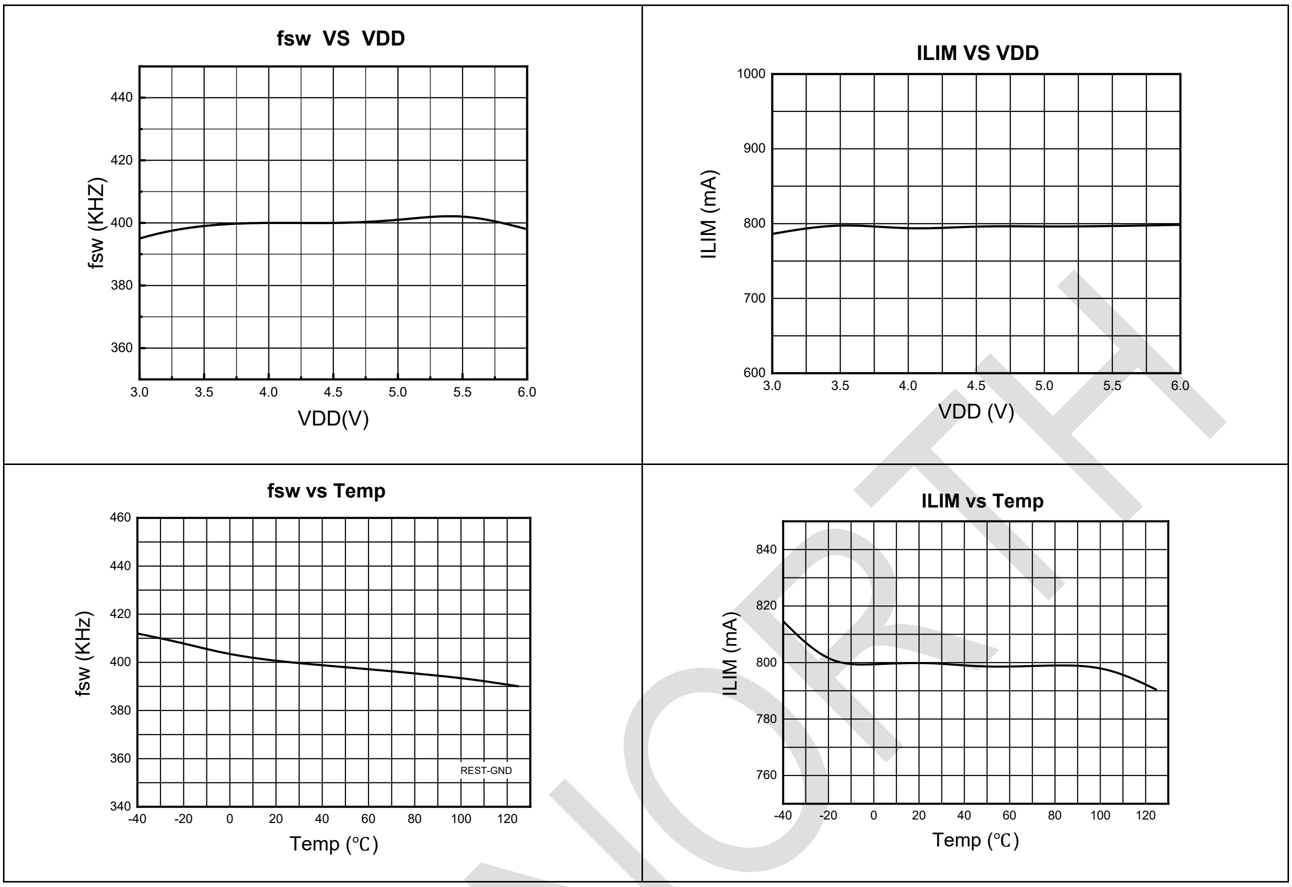
10.5 Electrical Characteristics

Test conditions: (V_{DD}=5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{DD}		2.8		9	V
Input undervoltage threshold	V_{UVLO}	VDD rising	2.3	2.5	2.7	V
Input Undervoltage Hysteresis	V_{UVLO_HYS}			200		mV
Input quiescent current	I_Q	C_{IN}=10uF，REST=float，EN=V_{DD}=5V		0.55	1	mA
Shutdown Current	I_{SHDN}	C_{IN}=10uF，REST=float，EN=0V		1		μA
Current Limit Protection	I_{LIM}	V_{D1}, V_{D2}, V_{DD} short	500	800		mA
EN Rising Threshold	V_{EN_H}	EN rising	1.3			V
EN falling threshold	V_{EN_L}	EN falling			0.4	V
VD1, VD2 pulse width mismatch ratio	DMM			0		%
Dead time	t_{BBM}			80		ns
Duty Cycle	Duty			50		%
On-resistance	R_{ON}			300		mΩ
Switching Frequency	fsw	REST=GND		360		KHz
		REST=5K		1790		KHz
		REST=150K		186		KHz
Thermal Shutdown Threshold	T_{SHDN}	T_A rising		160		°C
Thermal shutdown hysteresis	T_{SHDN_HYS}			30		°C

10.6 Characteristics Curve

(V_{DD}=5V, T_A=25°C, unless otherwise specified.)



11 Detailed Description

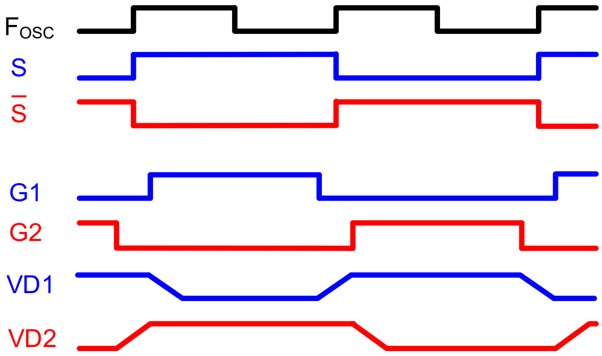
11.1 Overview

The CN3501TER is a 5V, 0.5A push-pull transformer driver. It integrates two N-channel power MOSFETs. It is specifically designed for low cost, small size, low EMI isolated DC/DC power supplies.

The chip includes an oscillator that powers the gate driver circuit. The gate driver circuit includes a divider and a break-before-break (BBM) logic that provides two complementary output signals that alternately turn on and off the two NMOSs, incorporating a period of dead time between turning the NMOSs on and off to avoid shorting out the ends of the transformer primary windings. The resulting output signals drive the isolation transformer and rectifier to convert the input voltage to an isolated output voltage.

The CN3501TER has a variety of protection features. The overcurrent protection helps to control the transformer current to avoid transformer saturation; when the junction temperature is higher than the thermal shutdown threshold, it will disconnect the NMOS to prevent the chip from being damaged by high temperature, and it also has an input UVLO to ensure stable operation.

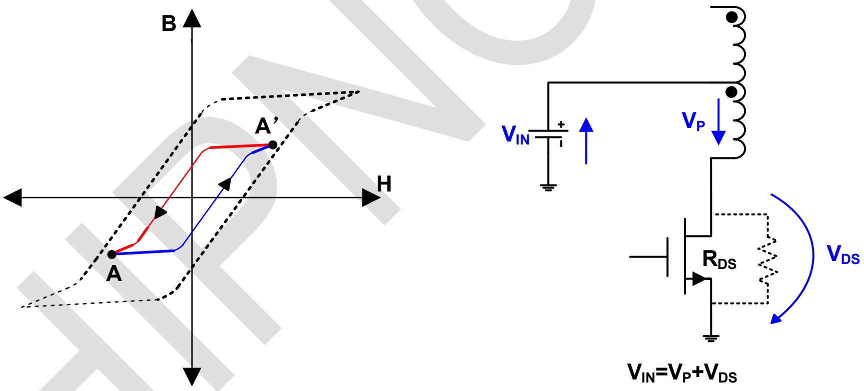
11.2 Push-Pull Converters



Driver Timing Diagram

G1 and G2 correspond to the logic level of the gate voltage of the power MOSFETs Q1 and Q2, their high level pulse width is the same, there is a period of time between the high level at the same time for the low level, the time for the dead time t_{BBM} to avoid the phenomenon of the two power MOSFETs of the common, as well as to realize the power MOSFETs in the lower leakage voltage turn on, reduce switching losses. Detect the gate voltage size of power MOSFETs Q1 and Q2 when they are turned off, and generate t_{BBM} only after the power MOSFETs are turned off to avoid driving delay and its temperature coefficient and affect the size of the dead time to ensure consistency in the application of the full input voltage range.

11.3 Core Magnetization



Push-pull transformer core magnetization curve

The figure above shows the ideal magnetization curve for a push-pull converter, where B is the flux density and H is the magnetic field strength. when Q1 is on, the flux is pushed from A to A', and when Q2 is on, the flux is pulled from A' back to A. The difference between the flux and the flux density is directly proportional to the product of the primary voltage, V_P, and the time t_{ON} that has been applied to the primary voltage: $B \approx V_P \times t_{ON}$. this volts-per-second (V-t) product is important, because it determines the core magnetization during each switching cycle. If the V-t product of the two phases is not the same, the flux density swings out of balance and away from the origin of the B-H curve. If equilibrium is not restored, the offset will increase with each subsequent cycle and the transformer will slowly move toward the saturation region. The output FET of the CN3501TER is self-correcting for V-t imbalance due to the positive temperature coefficient of the MOSFET on-resistance. With a slightly longer on-time, the prolonged current flow through the FET gradually heats up the transistor, resulting in an increase in RDS-on. The higher resistance causes the drain-source voltage VDS to rise. Since the primary voltage is the difference between the constant input voltage V_{IN} and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, V_P gradually decreases, and V-t returns to equilibrium.

11.4 Current clamp drive mode

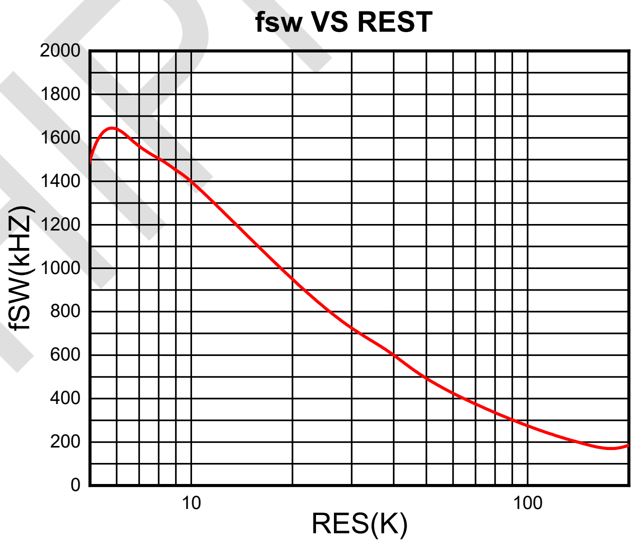
In the converter start-up phase, output short-circuit or transformer magnetic saturation, the current through the power MOSFET will be detected to be too large, then reduce the gate drive voltage of the power MOSFETs Q1 and Q2, to limit the size of the current to 0.8A, which not only ensures that the power MOSFET is in a safe operating area, but also makes the transformer and output rectifier diode from the impact of high current, improve the reliability of the converter.

11.5 Adjustable frequency

The CN3501TER has a wide switching frequency range from 200 kHz to 1.8 MHz, and the switching frequency can be set by connecting a resistor to GND via the REST pin. The following table lists the REST values required to achieve a specific operating frequency (f_{SW}).

The choice of switching frequency is a trade-off between efficiency and component size. For example, when operating at a higher switching frequency, the size of the transformer is reduced, resulting in a smaller design footprint and lower cost. However, higher frequencies increase switching losses, which reduces overall power supply efficiency.

REST	fsw
Floating	360K
200K	141K
50K	473K
20K	939K
5K	1790K
0Ω(short circuit to ground)	360K



11.6 Enabling control

Startup and shutdown are controlled by the EN pin and the VDD pin. To keep the chip in shutdown mode, a voltage lower than EN_L needs to be applied to the EN pin. If the EN pin voltage is higher than EN_H but the VDD voltage is still lower than VUVLO, the VD1 and VD2 switch nodes will not be activated, and the chip will start working once VDD is higher than VUVLO.

There are two ways to start the chip, the simplest way is to connect the EN pin to the VDD pin, when the VDD pin voltage is higher than VUVLO, the chip will start itself. The second method is to connect an external logic output to drive the EN pin, which allows you to customize the power-up timing.

11.7 Output short-circuit protection principle

CN3501TER output short-circuit protection is realized by current clamp driving mode and over-temperature protection. In the push-pull converter output short-circuit, the transformer primary winding is clamped to take the voltage drop is small, the input power supply VIN most of the voltage drop by the N-channel power MOSFETs Q1 or Q2 to take, when the detection of the power MOSFETs through the larger current, the chip enters the current clamp drive mode, due to the heat of the power MOSFETs resulting in the temperature of the chip rises to the trigger of the over-temperature protection. The lower the ambient temperature, or the lower the input voltage, the smaller the rate of temperature rise, will make the temperature rise to over-temperature protection for a longer period of time, so as to obtain the adaptive super-tolerant load capacity.

11.8 General mode of operation

In the start-up phase, due to the lower voltage of the converter output capacitor, the current of the power MOSFET is larger, then this phase is started in the current-clamped drive mode; when the converter output voltage reaches near the rated output voltage, the power MOSFET current is smaller, and the drive voltage is increased so that its conduction internal resistance is minimized.

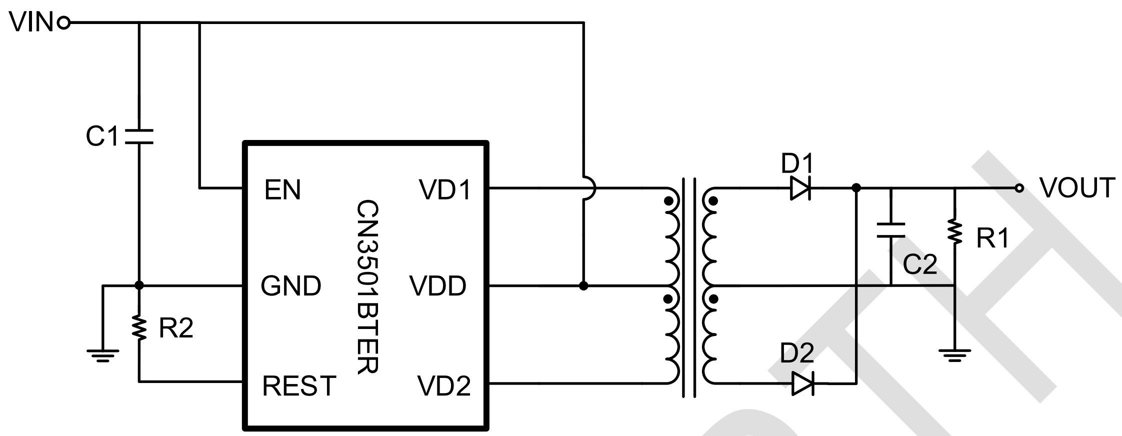
11.9 Over-temperature protection

CN3501TER internal integrated over-temperature protection, trigger threshold typical value of 160 ℃, when the chip junction temperature exceeds this temperature, the chip will enter the protection state, the oscillator stops working until the chip junction temperature is lower than the typical value of 130 °C, the chip back to normal operation.

12 Application Information

12.1 Typical Application

The following figure shows a typical application schematic for a circuit that can be used as a means of evaluating the performance of the CN3501TER.



Typical Application

12.2 Design Requirements

Requirement	Min	Typ	Max	Unit
5V output voltage		5		V
Input voltage		5		V
fsw		360		KHZ
IOUT		400		mA

12.3 Design process

12.3.1 Input Capacitance

The power input VDD should be grounded with a low ESR ceramic capacitor. Recommended capacitance values range from 1μF to 10μF, typically 10μF. The capacitors are rated at two times the input voltage and are made of X5R or X7R.

12.3.2 Output Capacitor

Push-pull converter can theoretically realize 100% duty cycle to the second side of the transmission of energy, but in order to ensure the reliable operation of the push-pull converter, MOS Q1 and Q2 switching process needs to reserve a certain amount of dead time, in order to prevent the emergence of common. During the dead time, the output energy is mainly provided by the output filter capacitor C2, so a certain amplitude of output ripple will be generated at this stage. In practice, capacitor C2 is recommended to use 4.7uF-10uF ceramic capacitors, which can bring better filtering effect for the converter.

12.3.3 Output Rectifier Diode

The output rectifier circuit is recommended to use Schottky diode with low on-state voltage drop and short reverse recovery time, which can bring better load regulation rate and higher conversion efficiency for push-pull converter. This application program uses the output full-wave rectifier circuit structure, the rectifier diode reverse voltage stress for the output voltage amplitude of two times, so the output rectifier diode reverse withstand voltage amplitude should be in accordance with the output voltage of the largest value (in the highest input voltage, the minimum load conditions) more than two times to ensure that the use of derating. Rectifier diode reverse withstand voltage calculation formula:

$$Diode\ V_R > 1.5 * 2 * \frac{N_S}{N_P} * V_{INMAX}$$

N_P is the number of turns of the primary winding of the push-pull transformer, N_S is the number of turns of the secondary winding of the push-pull transformer, and V_{INMAX} is the maximum input voltage.

Output rectifier diodes should be selected to meet the requirements of the actual operating temperature range of models, in particular, it should be noted that in the highest operating temperature conditions, Schottky diode reverse leakage current will increase significantly, so you need to be based on the diode's high-temperature operating characteristics of the reasonable use of the dosage, specific diode specifications can be viewed in the temperature derating curve. In order to ensure that the push-pull converter in any working conditions, reliable and stable operation, the output rectifier diode selection also need to consider the maximum operating current in the output side of the short-circuit anomaly.CN3501TER in the output of the short-circuit protection mode, the chip will automatically switch to the current clamp drive mode, the working current of the MOSFET will be limited to the current clamp limit value of ILIM (typical value of 0.8A), then The maximum operating current of the output rectifier diode can be derived from the transformer turns ratio relationship, which can be calculated by the following formula:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{LIM-MAX}$$

$I_{LIM-MAX}$ is the maximum value of the current limit.

In the output short-circuit protection mode, the CN3501TER will first switch to current clamp drive mode, with the chip's power consumption increases, will be triggered to enter the over-temperature protection state, the chip from the self-recovery process, to trigger the over-temperature protection to stop the work of the rectifier diode is in the state of the maximum operating current during this period of time, so the output rectifier diode should be selected to ensure that the peak forward surge current (IFSM-Forward current surge peak) can meet the requirements.

12.3.4 Push-pull transformer

Estimation of the turns ratio of the primary and secondary windings

Assuming that the output rectifier diode of the push-pull converter has been selected in accordance with the design requirements, and that the forward conduction voltage drop of the rectifier diode under maximum output load conditions is V_F, the turns ratio of the primary and secondary windings of the push-pull transformer can be estimated on the basis of the input voltage of the primary winding and the minimum output voltage of the secondary winding. Under nominal input and output full load conditions, the input voltage across the primary winding of the push-pull transformer is:

$$V_P = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times R_{DS(ON)}$$

Where P_{O-MAX} is the maximum output power of the push-pull converter, η is efficiency, the estimated conversion efficiency of the push-pull converter under full load conditions, and RDS(ON) is the on-resistance of the chip's built-in N-MOS. The output minimum voltage of the secondary winding under full load condition is:

$$V_S = V_{O-MIN} + V_F$$

V_{O-MIN} is the minimum voltage allowed to be output from the push-pull converter under full load conditions, in order to ensure that the output voltage characteristic curve meets the specifications under full load conditions, $V_{O\text{-}MIN}$ can be estimated at 97% of the nominal output voltage (-3% accuracy of the nominal output voltage), and V_F is the forward conduction voltage drop of the selected output rectifier diode under full load conditions. From the above formula can be derived from the original second-side winding turns ratio calculation formula:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times R_{DS(ON)}}{V_{O-MIN} + V_F}$$

With the input and output requirements of this application case, the turns ratio of the primary and secondary windings of the push-pull transformer can be estimated by assuming a conversion efficiency of 85% for the push-pull converter:

$$N_{PS} = \frac{5V - \frac{2W}{0.85 * 5V} * 0.3\Omega}{5V * 0.97 + 0.4V} \approx 0.93$$

Push-Pull Transformer Volt-Second Product Estimation

To prevent transformer saturation, the volt-second product of the selected push-pull transformer must be greater than the maximum volt-second product generated by the CN3501TER under all normal operating conditions. In narrow input isolated power applications, ±10% of the nominal input voltage is usually specified as the input range of the power supply, so the volt-second product of the push-pull transformer should be calculated according to the upper limit of the input voltage of the power supply. The frequency and tolerance set by the chip itself should also be considered to meet the minimum operating frequency conditions without saturation. The maximum volt-second product applied to the primary winding of the transformer by the CN3501TER is generated under the condition of half of the switching period corresponding to the set minimum operating frequency and the maximum input voltage. Therefore, the following calculation method can be used to estimate the minimum volt-second product of a push-pull transformer:

$$Vt_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

With the design requirements of this application case, assuming a set operating frequency typical of 360 KHz and a minimum operating frequency of 300 KHz, the volt-second product of the selected push-pull transformer should be satisfied under the highest input conditions:

$$Vt_{MIN} \geq \frac{5V \times 110\%}{2 \times 300KHZ} \approx 9V\mu s$$

The selection of push-pull transformers should be based on the actual application requirements to find the appropriate size of the volt-second product and the turns ratio of the original and secondary windings, while the maximum output power, isolation voltage level, isolation distribution capacitance should also be used as an important reference basis for the selection of push-pull transformers.

12.4 Bill of materials

Symbol	Description	Manufactures	Part Number
T1	N1:N2:N3:N4=1:1:1.11:1.11, Volt-second product:11.4Vus		
C1，C2	10uF±10%，25V，X5R，0603	muRata	GRM188R61E106KA73D
R2	3.9K±1%，0603	UNI-ROYAL	0603WAF3901T5E
D1，D2	VF：470mV@1A，IF：1A，VR：30V，IR：60uA@30V	Onsemi	MBR130T1G

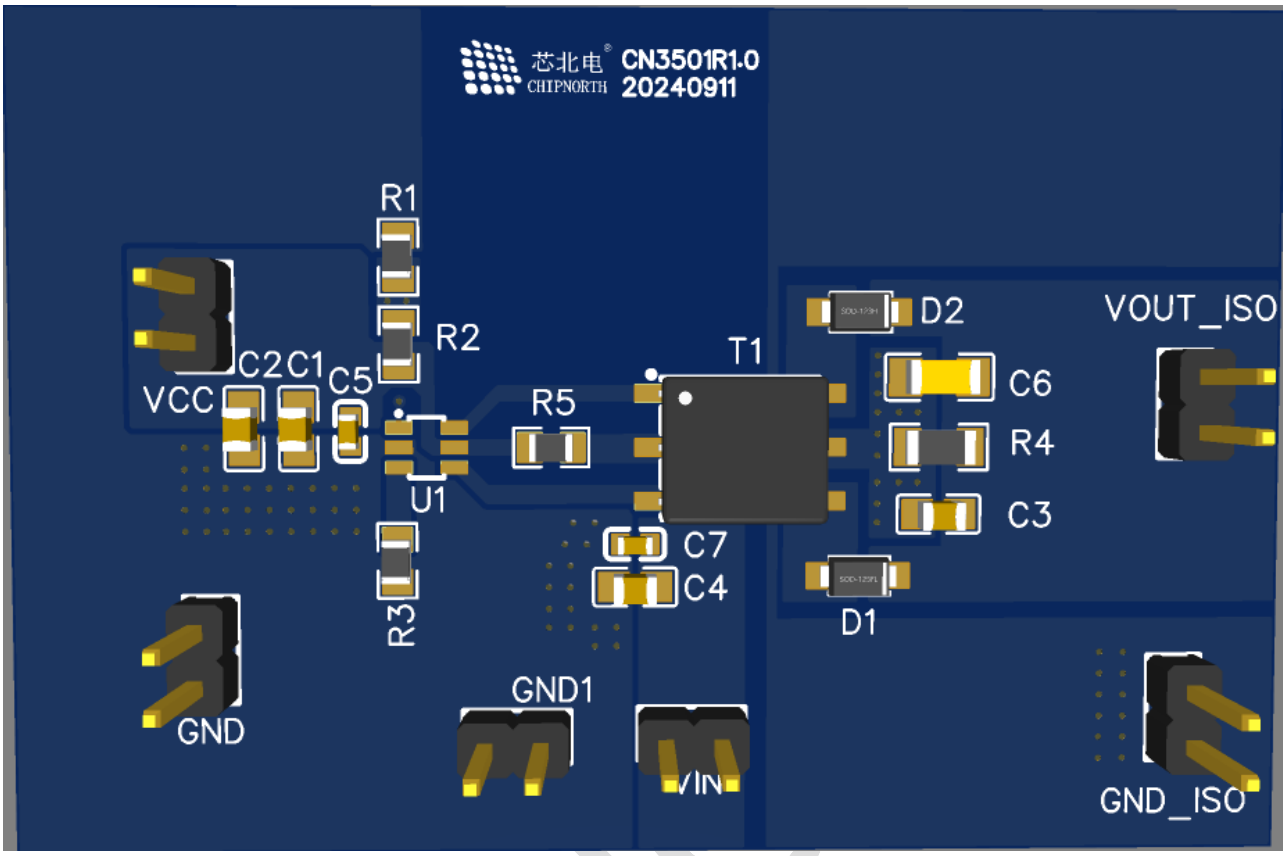
12.5 PCB Layout Guidelines

For all switching power supplies, the layout is an important step, especially in the case of high peak currents and high frequencies, and the careful layout may affect the stability of the converter and electromagnetic interference. Here are some suggestions for place-and-route:

12.5.1 BUCK Converter

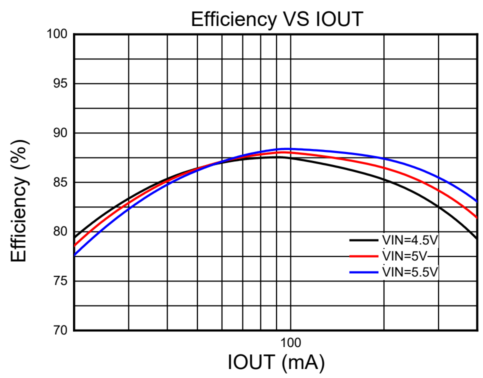
- The VDD capacitor is placed as close as possible to the chip VDD and GND pins to minimize the loop area formed by the input capacitors, VDD and GND pins.
- For reliable operation, it is recommended to use a 0.1μf low ESR ceramic bypass capacitor at the VDD pin of the device. In the PCB layout, the capacitor should be as close as possible to the power supply pins and on the same layer. The capacitors must be rated for a voltage greater than the VIN voltage rating.
- The connections between the VD1 and VD2 pins and the transformer primary terminals and between the VIN pin and the transformer center tap must be as short as possible to minimize parasitic inductance.
- The connection between the VIN pin and the transformer center tap needs to be grounded with a low ESR ceramic capacitor. Recommended capacitance values range from 1 μF to 10 μF, generally 10 μF. The capacitor voltage rating must be greater than the VIN voltage rating, and it is recommended to use X5R or X7R material capacitors.
- The device's GND pin is recommended to be connected to the PCB ground plane using two via holes to help minimize inductance.
- Capacitors and other connections to ground plane should use two vias to minimize inductance.
- Rectifier diodes should be Schottky diodes with low forward voltage and low capacitance to maximize efficiency.
- The VOUT pin shall be connected to ISO ground with a low ESR ceramic capacitor. Typical capacitance values are 4.7μF ~ 10μF, 10μF is recommended.

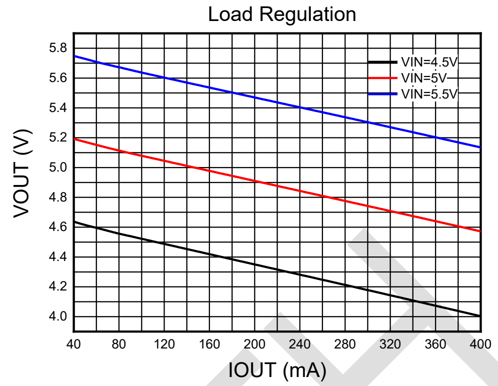
12.5.2 Layout


芯北电 CHIPNORTH CN3501R1.0 20240911
R1
R2
VCC
C2
C1
C5
U1
R5
T1
R3
D2
VOUT_ISO
C6
R4
C3
C7
C4
D1
GND
GND1
VIN
GND_ISO

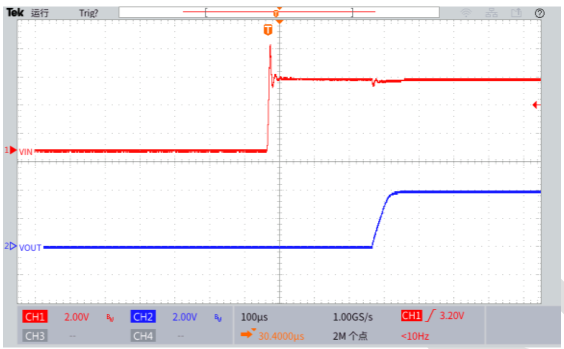
12.6 Basic Performance

Note: 5-5V application operating circuit

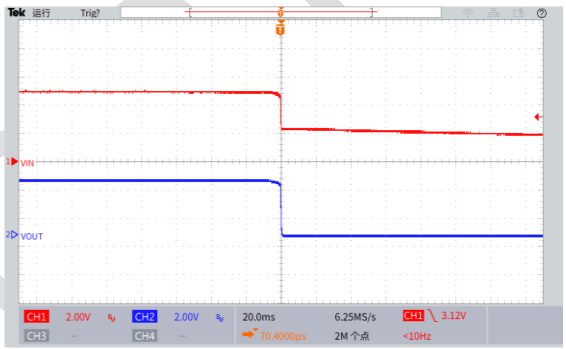




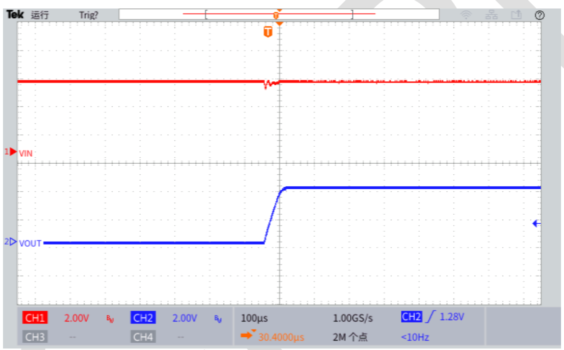
12.7 Operating Waveforms



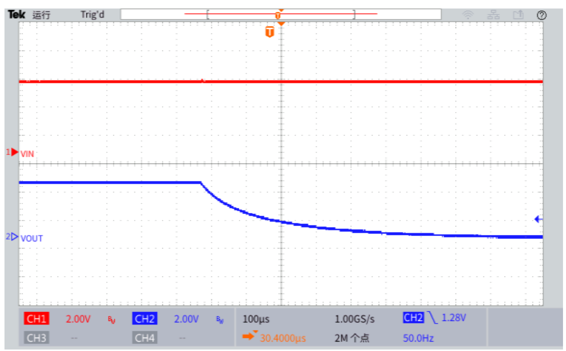
V_{IN}=0-5V，V_{EN}=5V，V_{OUT}=5V/250mA



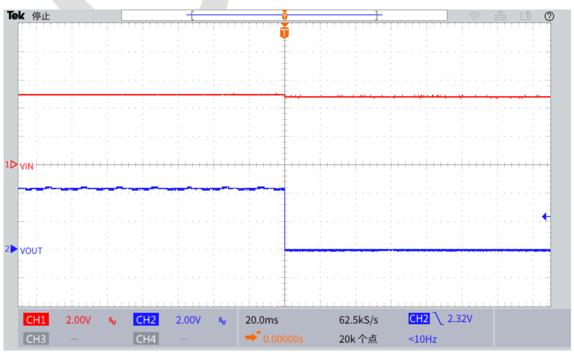
V_{IN}=5-0V，V_{EN}=5V，V_{OUT}=5V/250mA



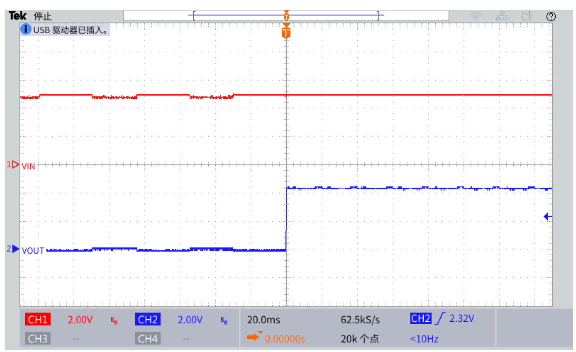
V_{IN}=5V，V_{EN}=0-5V，V_{OUT}=5V/250mA



V_{IN}=5V，V_{EN}=5-0V，V_{OUT}=5V/250mA



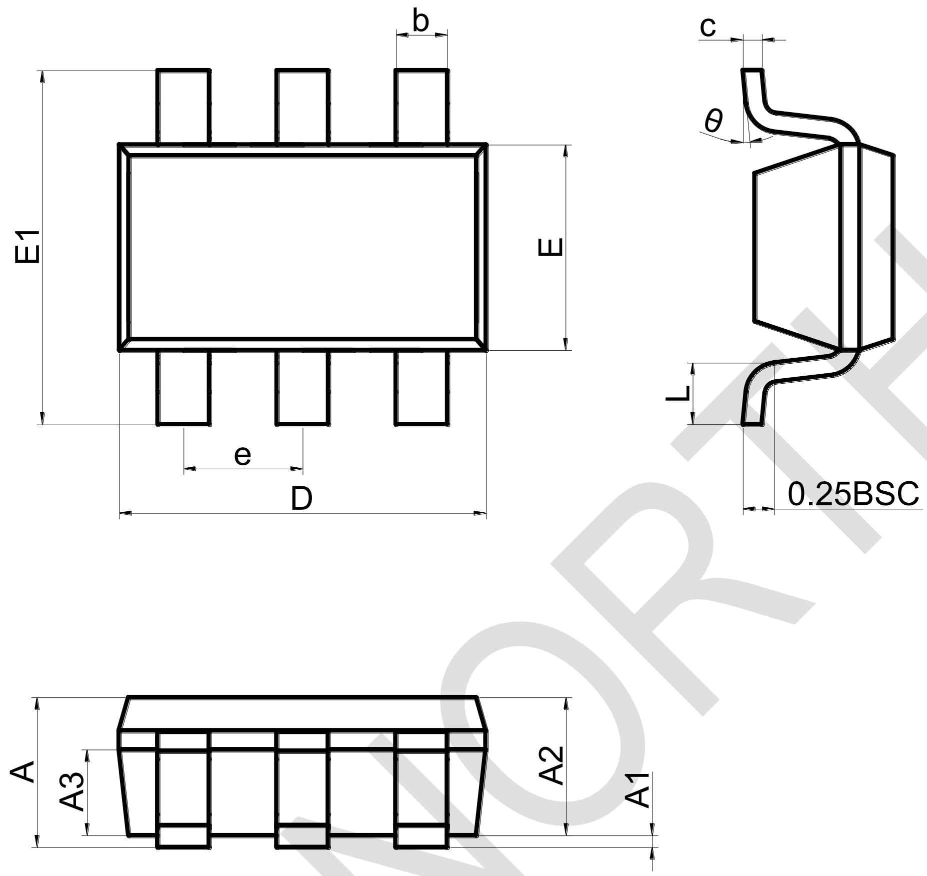
short circuit on power up



Short circuit recovery

13 Package Information

SOT23-6



Symbol \ Dimension	Min (mm)	Nom (mm)	Max (mm)
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E	1.510	1.610	1.700
E1	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

14 Important Statement

Chipnorth Electronic Technology (Nanjing) Co., Ltd. and its subsidiaries reserve the right to make modifications, improvements, corrections, or other changes to this document and to any of the products described herein at any time without notice. Chipnorth Electronic Technology (Nanjing) Co., Ltd. disclaims any liability arising out of the use of this document or any of the products described herein; Chipnorth Electronic Technology (Nanjing) Co., Ltd. does not transfer any license to its patents or trademarks or other rights. Any customer or user using this document or any of the products described herein assumes all risk and agrees to hold harmless Chipnorth Electronic Technology (Nanjing) Co., Ltd. and all companies whose products are displayed on Chipnorth Electronic Technology (Nanjing) Co., Ltd.

Chipnorth Electronic Technology (Nanjing) Co., Ltd. makes no warranty and assumes no responsibility for any products purchased through unauthorized sales channels. In the event that a customer purchases or uses a product from Chipnorth Electronic Technology (Nanjing) Co., Ltd. for any unintended or unauthorized use, the customer shall indemnify and hold harmless Chipnorth Electronic Technology (Nanjing) Co., Ltd. and its representatives from and against all claims, damages, and attorney's fees arising from any personal injury or death, directly or indirectly, arising out of or in connection with such purchase or use.