4COM Segment type LCD Driver 6uA typ.

1 Description

The CN91C4S96 is a segment-type LCD driver chip with a duty cycle of 1/4, capable of driving up to 384 segments. This device incorporates a low-power design, enabling it to achieve ultra-low power consumption and reduce power loss from the power supply.

2 Features

- Fixed 1/4 duty mode, Up to 384 dots
- Low power consumption design, 6uA current at typical condition
- Built-in OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Interface: 2 line serial I2C
- Compatible with TTL/CMOS
- High EMC immunity

3 Applications

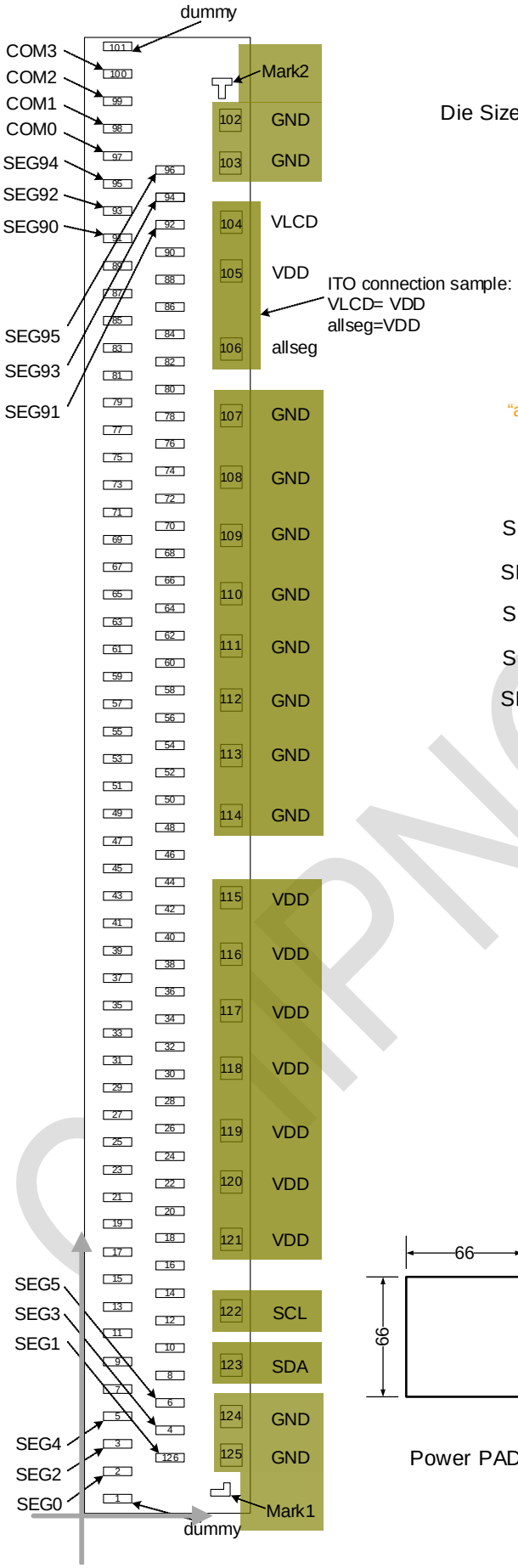
- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

4 Order Information

Product Number	Package	Quantity
CN91C4S96	COG	154/Tray

5 PAD Description

Name	I/O	Function
SDA	I/O	2-line serial I2C, data input and output
SCL	I	Open-Drain, and a pull-up resistor on board is needed.
VSS	I	GND
VDD	I	Power
VLCD	I	Set LCD bias voltage. It can be directly tied to VDD, and then you can adjust the internal LCD bias voltage by setting the register EV[3:0]. The voltage applied to VLCD pin must be equal to or lower than VDD.
allseg	I	Should be directly tied to VDD
SEG0~SEG95	O	SEGMENT driver output for LCD
COM0~COM3	O	COMMON driver output for LCD



Die Thickness: 300um

Die Size(without scribe lane): 4300um X 500um

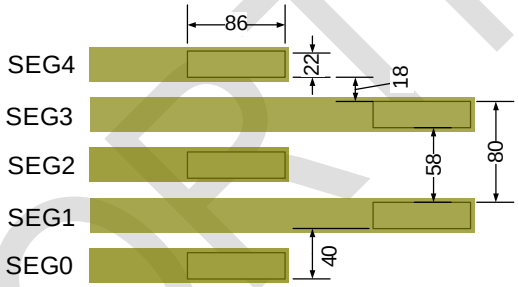
Bump Hight: 9um ± 2um

SEG Bump Width: 22um

SEG Bump Space: 18um

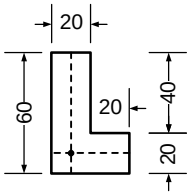
SEG Bump Pitch: 40um

"allseg" PAD is very important, it defines the SEG ITO pitch.
Please refer to the SEG ITO samples as follows:

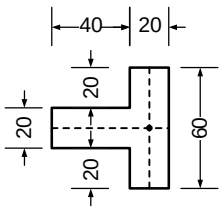


(allseg=VDD)

Power PAD



Mark1



Mark2

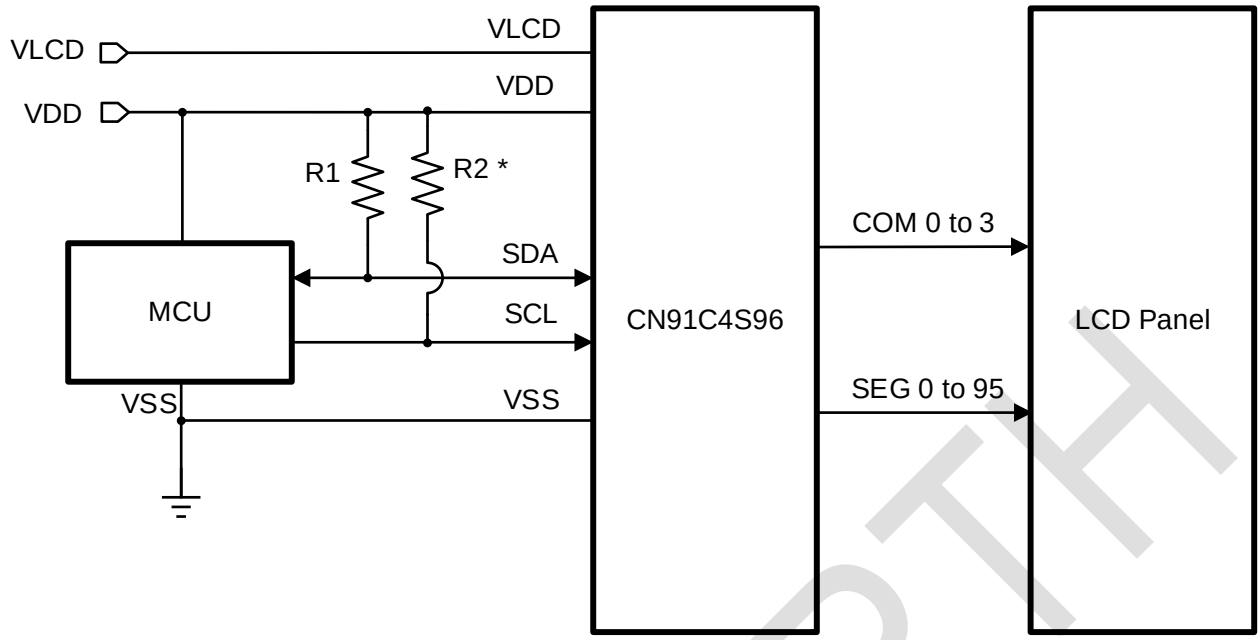
6 PAD Coordinates for COG

UNIT： μm

No	Name	X	Y	No	Name	X	Y
1	dummy	110	30	39	SEG38	110	1630
2	SEG0	110	110	40	SEG39	272	1670
3	SEG2	110	190	41	SEG40	110	1710
4	SEG3	272	230	42	SEG41	272	1750
5	SEG4	110	270	43	SEG42	110	1790
6	SEG5	272	310	44	SEG43	272	1830
7	SEG6	110	350	45	SEG44	110	1870
8	SEG7	272	390	46	SEG45	272	1910
9	SEG8	110	430	47	SEG46	110	1950
10	SEG9	272	470	48	SEG47	272	1990
11	SEG10	110	510	49	SEG48	110	2030
12	SEG11	272	550	50	SEG49	272	2070
13	SEG12	110	590	51	SEG50	110	2110
14	SEG13	272	630	52	SEG51	272	2150
15	SEG14	110	670	53	SEG52	110	2190
16	SEG15	272	710	54	SEG53	272	2230
17	SEG16	110	750	55	SEG54	110	2270
18	SEG17	272	790	56	SEG55	272	2310
19	SEG18	110	830	57	SEG56	110	2350
20	SEG19	272	870	58	SEG57	272	2390
21	SEG20	110	910	59	SEG58	110	2430
22	SEG21	272	950	60	SEG59	272	2470
23	SEG22	110	990	61	SEG60	110	2510
24	SEG23	272	1030	62	SEG61	272	2550
25	SEG24	110	1070	63	SEG62	110	2590
26	SEG25	272	1110	64	SEG63	272	2630
27	SEG26	110	1150	65	SEG64	110	2670
28	SEG27	272	1190	66	SEG65	272	2710
29	SEG28	110	1230	67	SEG66	110	2750
30	SEG29	272	1270	68	SEG67	272	2790
31	SEG30	110	1310	69	SEG68	110	2830
32	SEG31	272	1350	70	SEG69	272	2870
33	SEG32	110	1390	71	SEG70	110	2910
34	SEG33	272	1430	72	SEG71	272	2950
35	SEG34	110	1470	73	SEG72	110	2990
36	SEG35	272	1510	74	SEG73	272	3030
37	SEG36	110	1550	75	SEG74	110	3070
38	SEG37	272	1590	76	SEG75	272	3110

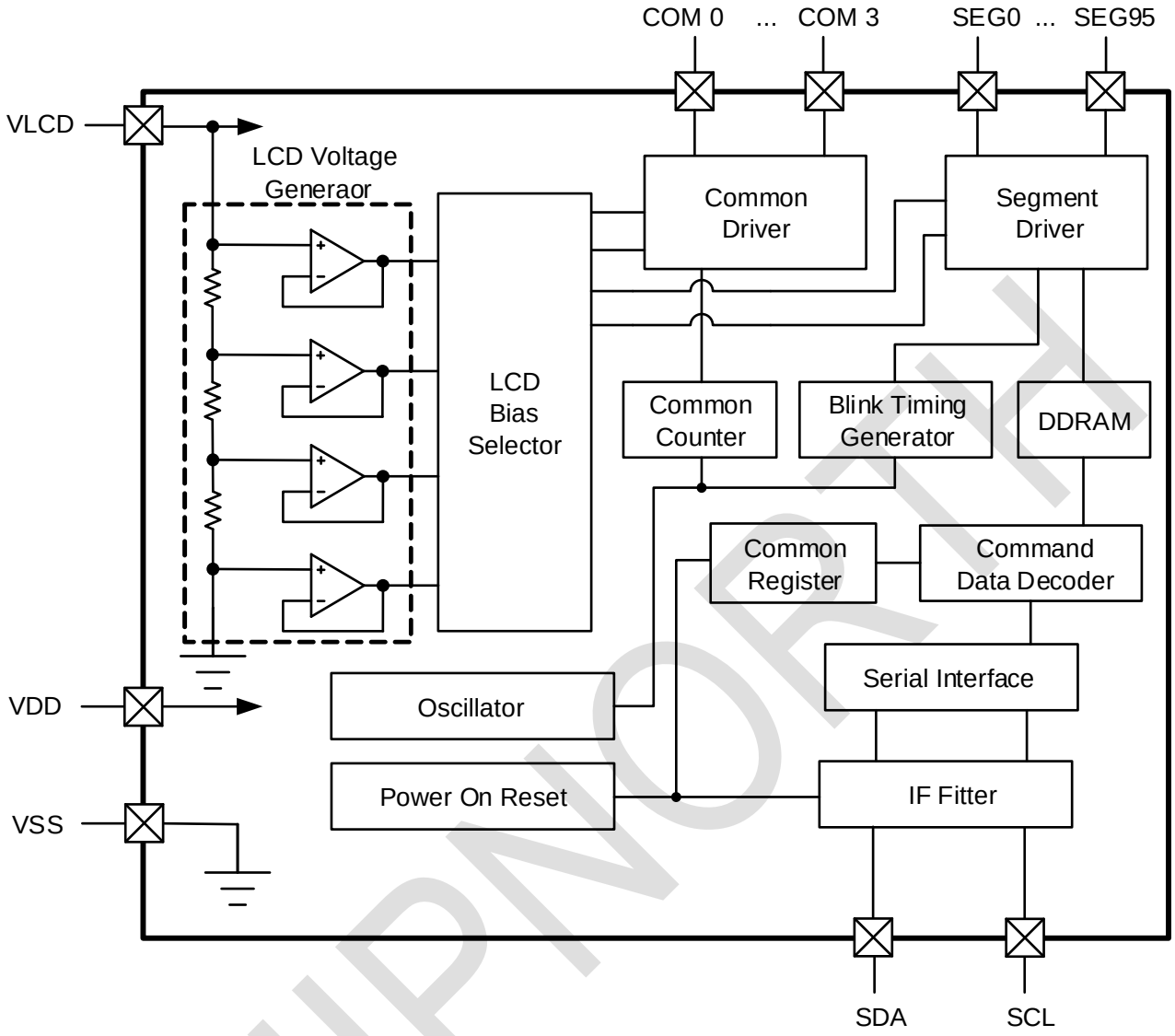
No	Name	X	Y	No	Name	X	Y
77	SEG76	110	3150	102	GND	444	4140
78	SEG77	272	3190	103	GND	444	4020
79	SEG78	110	3230	104	VLCD	444	3797
80	SEG79	272	3270	105	VDD	444	3637
81	SEG80	110	3310	106	allseg	444	3435
82	SEG81	272	3350	107	GND	444	3224
83	SEG82	110	3390	108	GND	444	3064
84	SEG83	272	3430	109	GND	444	2904
85	SEG84	110	3470	110	GND	444	2744
86	SEG85	272	3510	111	GND	444	2584
87	SEG86	110	3550	112	GND	444	2424
88	SEG87	272	3590	113	GND	444	2264
89	SEG88	110	3630	114	GND	444	2104
90	SEG89	272	3670	115	VDD	444	1860
91	SEG90	110	3710	116	VDD	444	1700
92	SEG91	272	3750	117	VDD	444	1540
93	SEG92	110	3790	118	VDD	444	1380
94	SEG93	272	3830	119	VDD	444	1220
95	SEG94	110	3870	120	VDD	444	1060
96	SEG95	272	3910	121	VDD	444	900
97	COM0	110	3950	122	SCL	444	670
98	COM1	110	4030	123	SDA	444	490
99	COM2	110	4110	124	GND	444	280
100	COM3	110	4190	125	GND	444	160
101	dummy	110	4270	126	SEG1	272	150
	Mark1	434	54		Mark2	414	4246

7 Typical Application



Note: * R2 is optional.

8 Block Diagram



9 Specifications

9.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3 to +6.5	V	Power supply
Power Supply Voltage 1	V_{LCD}	-0.3 to +V_{DD}	V	LCD drive voltage
Input voltage range	V_{IN}	-0.3 to V_{DD}+0.3	V	
Soldering Temperature	T_{lead}	260（soldering，10s）	°C	
Operational temperature range	T_{opr}	-40 to 105	°C	
Storage temperature range	T_{stg}	-55 to 150	°C	

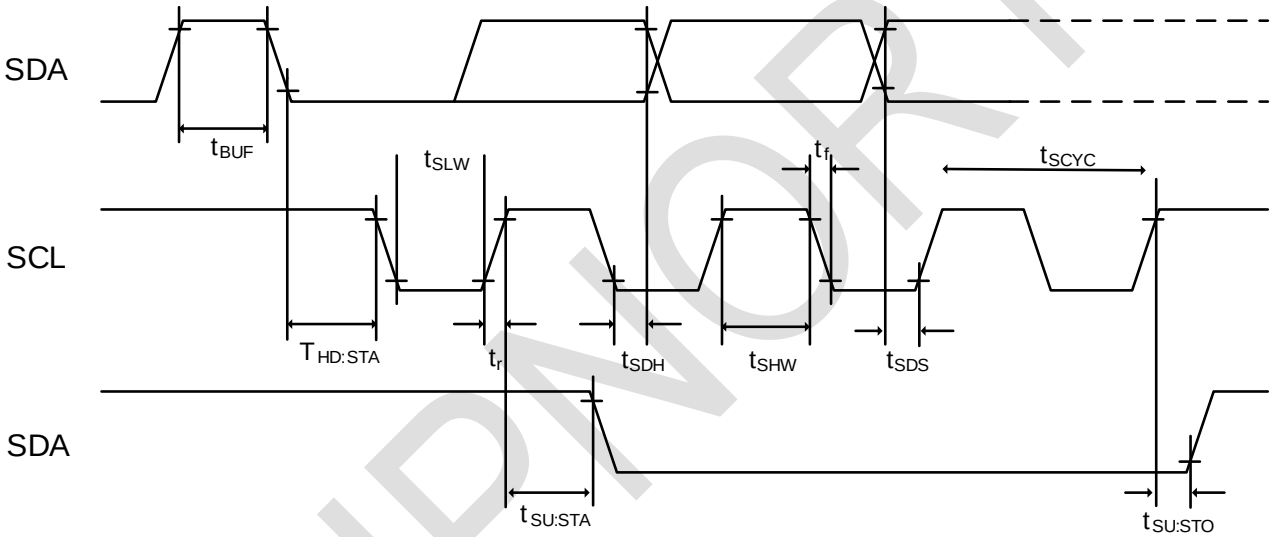
9.2 Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD Power Range	V_{DD}		2.7	-	5.5	V
VLCD Power Range	V_{LCD}	LCD drive voltage	2.7	-	V_{DD}	V
“H” Level Input Voltage	V_{IH}		0.8V_{DD}	-	V_{DD}	V
“L” Level Input Voltage	V_{IL}		V_{SS}	-	0.2V_{DD}	V
SDA "L" Level Output Voltage	V_{OL_sda}	I_{Load}=-3mA Without the consideration of ITO resistance on COG panel.	0	-	0.4	V
COM/SEG ON Resistance	R_{ON}	I_{Load}=±10uA	-	3	-	kΩ
Frame Frequency	F_{clk}	FR=72Hz setting	-	72	-	Hz
Standby Current	I_{DD1}	Display off, Oscillation off	-	-	1	uA
Operating Current	I_{DD2}	VDD=3.3V, Ta=25℃, SR=Power save mode 1, Frame inversion, FR=72Hz.	-	6	20	uA

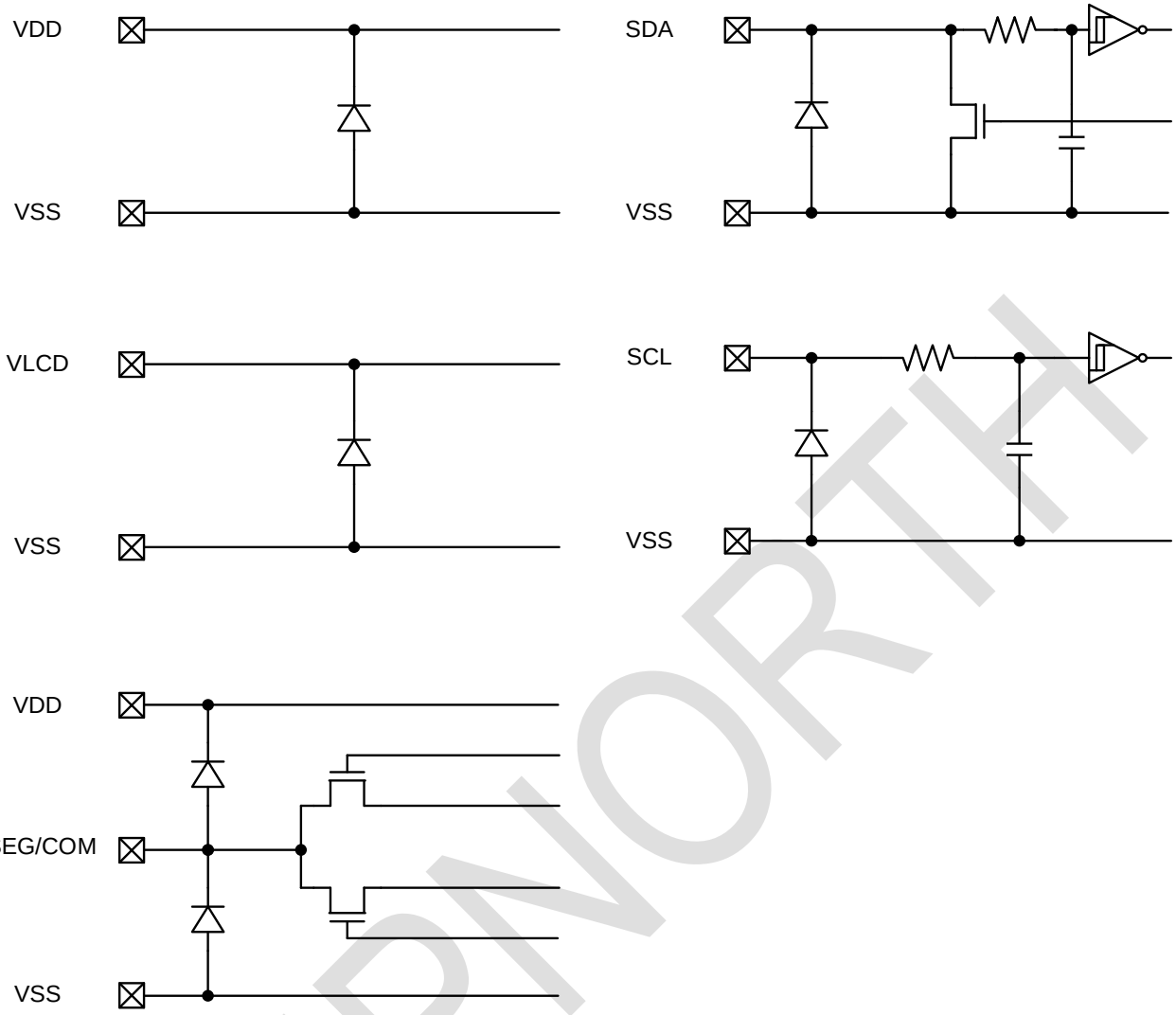
9.3 MPU Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Rise Time	t_r		-	-	1000	ns
Input Fall Time	t_f		-	-	300	ns
SCL Cycle Time	t_{SCYC}		10	-	-	us
“H” Level SCL Pulse Width	t_{SHW}		4	-	-	us
“L” Level SCL Pulse Width	t_{SLW}		4.7	-	-	us
SDA Setup Time	t_{SDS}		250	-	-	ns
SDA Hold Time	t_{SDH}		250	-	-	ns
Bus Free Time	t_{BUF}		4.7	-	-	us
START Condition Hold Time	$t_{HD;STA}$		4	-	-	us
START Condition Setup Time	$t_{SU;STA}$		4.7	-	-	us
STOP Condition Setup Time	$t_{SU;STO}$		4	-	-	us



2-line serial interface timing

10 Equivalent circuit of input and output



11 Command Registers Description

	7	6	5	4	3	2	1	0
ADSET	**C**	**0**	**0**	P[4:0]				
DISCTL	**C**	**0**	**1**	FR[1:0]		LF	SR[1:0]	
MODSET	**C**	**1**	**0**	ULP	EN	/	/	/
EVRSET	**C**	**1**	**1**	**0**	**0**	EV[2:0]		
ICSET	**C**	**1**	**1**	**0**	**1**	P[5]	RST	P[6]
BLKCTL	**C**	**1**	**1**	**1**	**0**	BF[2:0]		
APCTL	**C**	**1**	**1**	**1**	**1**	EV[3]	AON	AOFF

Name	Default	Description
P[6:0]	0000000	DDRAM Address. In the write mode, the range of address P [6:0] can be set as 0~5F(Hex). In the read mode, the range of address P [6:0] can be set as 0~62(Hex). Don't specify another address, otherwise address will be set to "0000000". Note: The P[5] and P[6] are in the command 'ICSET'.
FR[1:0]	00	Set Frame Frequency for Power Saving. 00, 72Hz, Normal Mode 01, 96Hz Operating Mode1 10, 49Hz, Operating Mode 2 11, 144Hz, Operating Mode 3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value 11, *1.8, High Power Mode
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	0: disable all blocks on-chip, all com/seg pin will be pulled to GND. 1: enable
EV[3:0]	0000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * VLCD 0001, 0.975 * VLCD 0010, 0.950 * VLCD 0011, 0.925 * VLCD 0100, 0.900 * VLCD 0101, 0.875 * VLCD 0110, 0.850 * VLCD 0111, 0.825 * VLCD 1000, 0.800 * VLCD 1001, 0.775 * VLCD 1010, 0.750 * VLCD 1011, 0.725 * VLCD 1100, 0.700 * VLCD 1101, 0.675 * VLCD 1110, 0.650 * VLCD 1111, 0.625 * VLCD Note: The bit EV[3] is in the command 'APCTL'.
RST	0	Set '1' to reset all the registers in this table, but it won't reset the display data in the DDRAM.
BF[2:0]	000	Config the blink frequency. 000, No blink.

		001, 0.3Hz 010, 0.25Hz 011, 2Hz 100~111, 1Hz
AON: AOFF	00	Config the pixel display. 00, All pixels are ON/OFF depending on the data in the display DDRAM. 01, All pixels are OFF regardless of DDRAM data. 10, All pixels are ON regardless of DDRAM data. 11, All pixels are OFF regardless of DDRAM data, the same as '01'.

12 Function Description

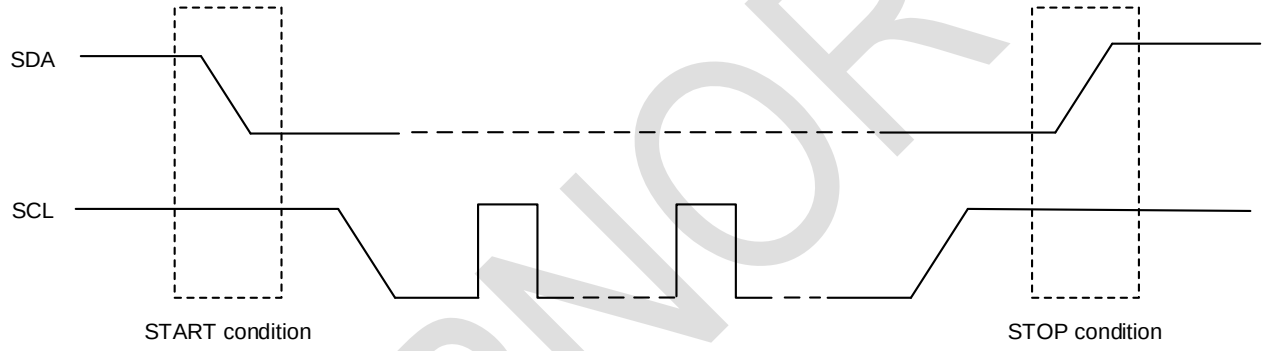
12.1 Command and Data Transfer Method

This Device is transfer data by 2-line serial interface.

When input command or data by 2-line serial interface, it must be generated the state of "START condition" and "STOP condition".

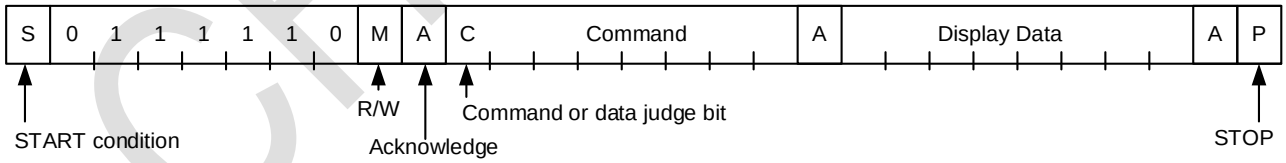
When set SDA "H"→"L" in SCL="H", it become "START condition".

When set SDA "L"→"H" in SCL="H", it become "STOP condition"



START condition and STOP condition.

1. Generate "START condition".
2. Issue Slave address 0x7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"

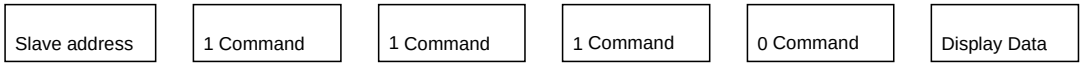


Issue the Slave Address ("01111100" for Write Mode or "01111101" for Read Mode) after the "START condition" is generated. Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation to be done is Write or Read operation.

The MSB (command or data judgment bit) defines if the succeeding byte is a command or data.

When "command or data judgment bit" ='1', the next byte is a command.

When "command or data judgment bit" ='0', the next byte is display data.



Once it enters display data transfer condition, it cannot input any command.

To input command again, please generate the “START condition” again.

If “START condition” or “STOP condition” is inputted in the middle of command transmission, the command will be cancelled. If the Slave address is continuously inputted following “START condition”, it will be in command input condition.

Please input “Slave Address” in the first data transmission after “START condition”.

When Slave Address cannot be recognized in the first data transmission, Acknowledge does not return and the next transmission will be invalid. When data transmission is in invalid status and the “START condition” is transmitted again, it will return to valid status.

Note: Please confirm that MPU Interface characteristic of Input rise/fall time and setup/hold time in transferring command and data meet the AC specifications. Refer to “MPU Interface Characteristics”.

12.2 Write Display Data and Transfer Method

Set R/W bit to ‘0’ to come into write mode.

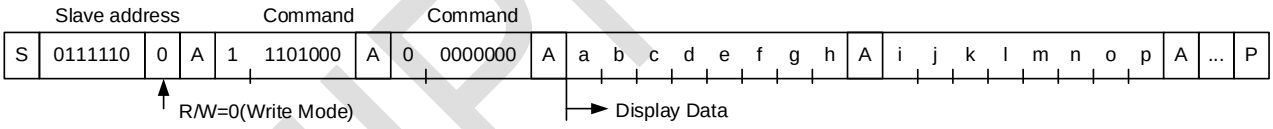
This device has Display Data RAM (DDRAM) of 96×4=384bit.

DDRAM address

BIT	00h	01h	02h	03h	04h	05h	06h	07h	……	5Dh	5Eh	5Fh	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	……	SEG93	SEG94	SEG95	

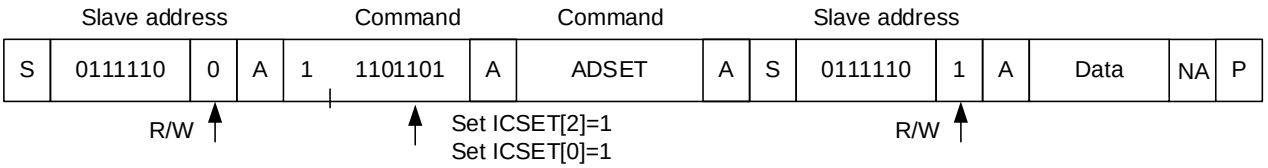
8bit data will be stored in DDRAM. The address to be written is the address specified by Address set command (ADSET), and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.



12.3 Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data read sequence.

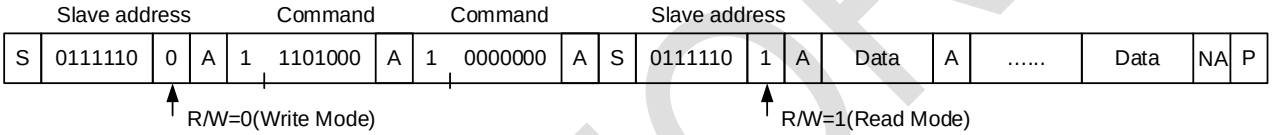


The command register addresses are described below. The following register settings can be read in this mode.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			60h
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOFF	61h
REG3	/	/	/	ULP	EV[3:0]				62h

12.4 Read Display Data and Transfer Method

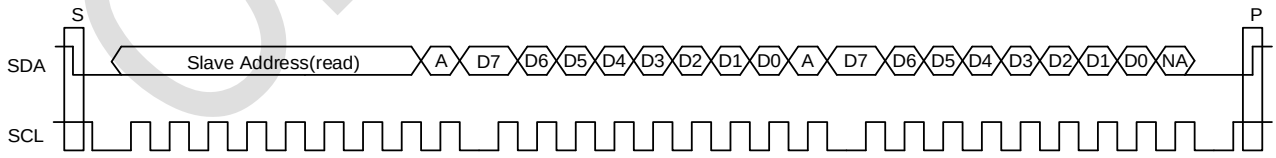
The read mode sequence is shown below.



During read mode, the display data can be read from the DDRAM through the SDA line. The data is outputted serially with SCL input. A write sequence is done first to identify the DDRAM address to be accessed. Then a “START condition” is transmitted again before entering the actual reading of DDRAM data and the Slave Address follows. The display data is outputted continuously afterwards. If no DDRAM address was specified right before the DDRAM read, the output during read mode will be from the current DDRAM address.

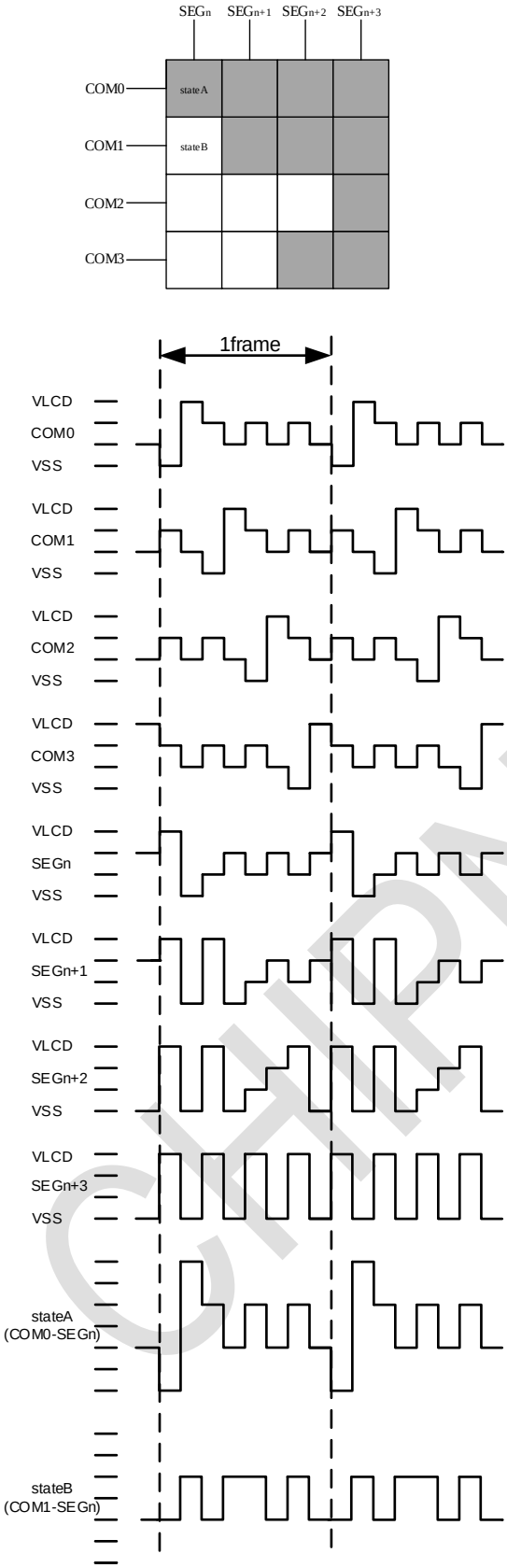
The DDRAM address will increment after every 8-bits of output data. An Acknowledge after every 8-bit of data outputted should be received from the master receiver. This will signal the device that it should continue to output the display data and increment the address. When Non-Acknowledge is received, the device will release the SDA line and the master can then transmit the “STOP condition”. The read mode will be finished once the “STOP condition” is received.

An example of the display data read sequence is shown below.

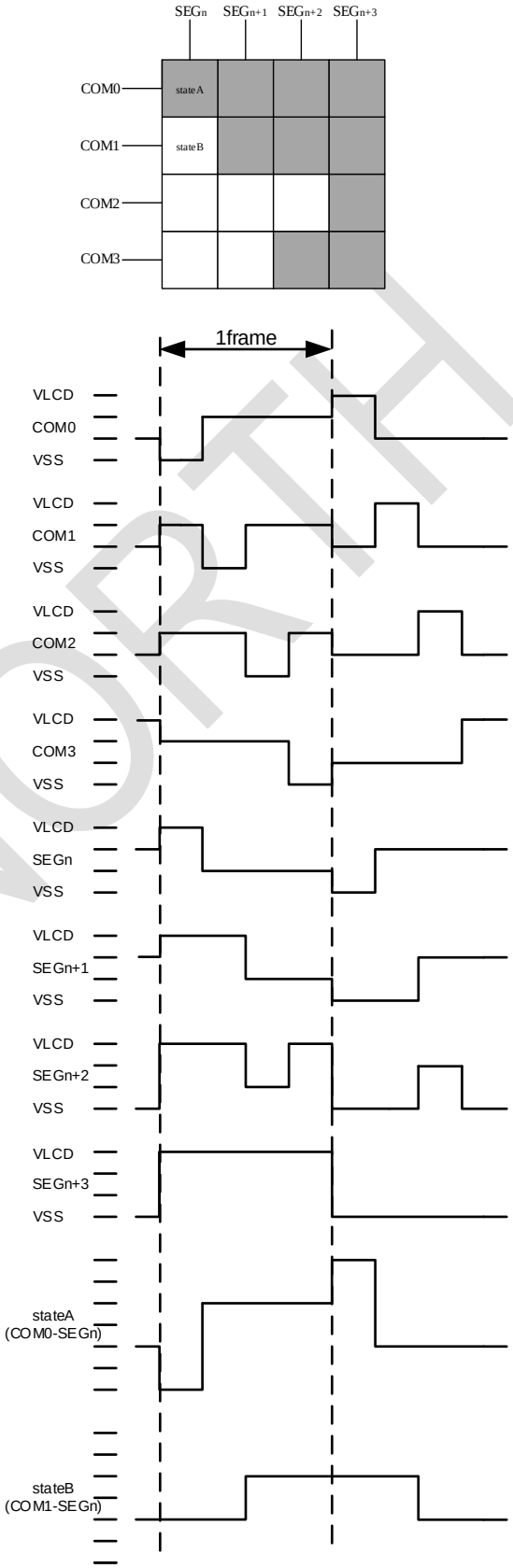


12.5 LCD Driving Waveform

Line Inversion Mode



Frame Inversion Mode



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