RAM Mapping 32×4LCD Controller for I/O MCU

1 Description

The CN9101C4S32 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the CN9101C4S32 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the CN9101C4S32. The CN9101C4S32 contains a power down command to reduce power consumption.

2 Features

- Operating voltage: 2.4V~5.5V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- R/W address auto increment
- VLCD pin for adjusting LCD operating voltage

3 Application

- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks
- Intelligent furniture

4 Ordering information

Product Number	Package	Quantity/Tape
CN9101C4S32	SSOP48	30/Tube
CN9101C4S32L	LQFP48	250/Tray
CN9101C4S32M	LQFP44	160/Tray
CN9101C4S32S	SOP28	25/Tube
CN9101C4S32P	SOP24	30/Tube
CN9101C4S32G	COG	TBD
CN9101C4S32B	COB	50/Tray

5 Marking

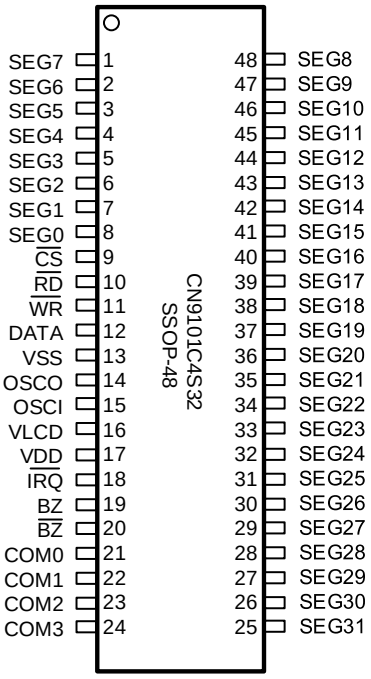
Product Number	Marking
CN9101C4S32	CN9101C4S32 GGYYWW
CN9101C4S32L	CN9101C4S32 GGYYWW
CN9101C4S32M	CN9101C4S32 GGYYWW
CN9101C4S32S	CN9101C4S32 GGYYWW
CN9101C4S32P	CN9101C4S32 GGYYWW

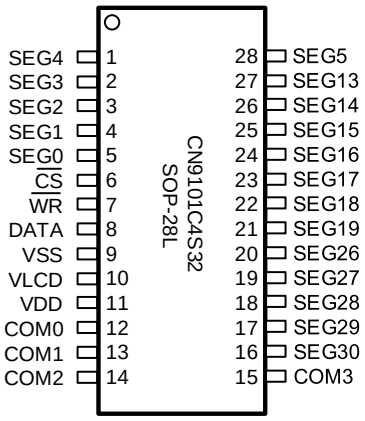
Note: YY=Year WW=Week.

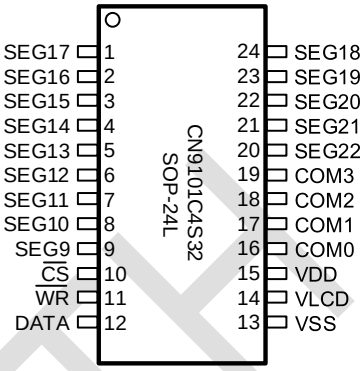
Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

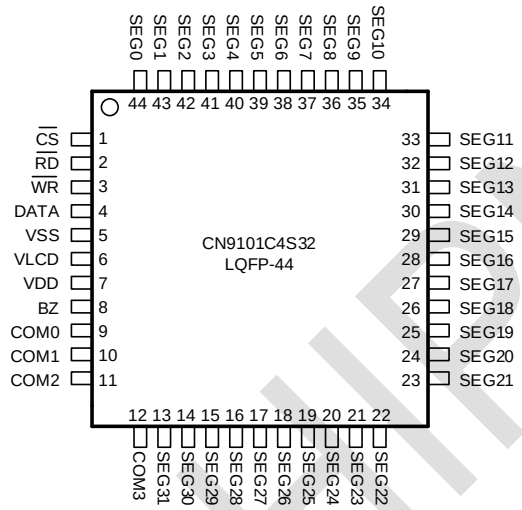
Moisture sensitivity level(MSL):3

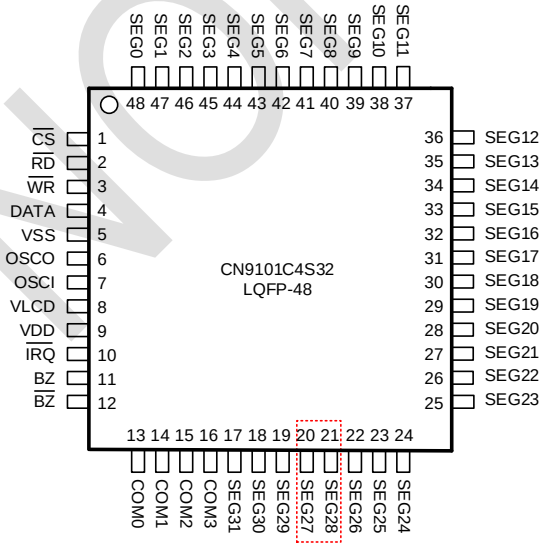
6 Pinout





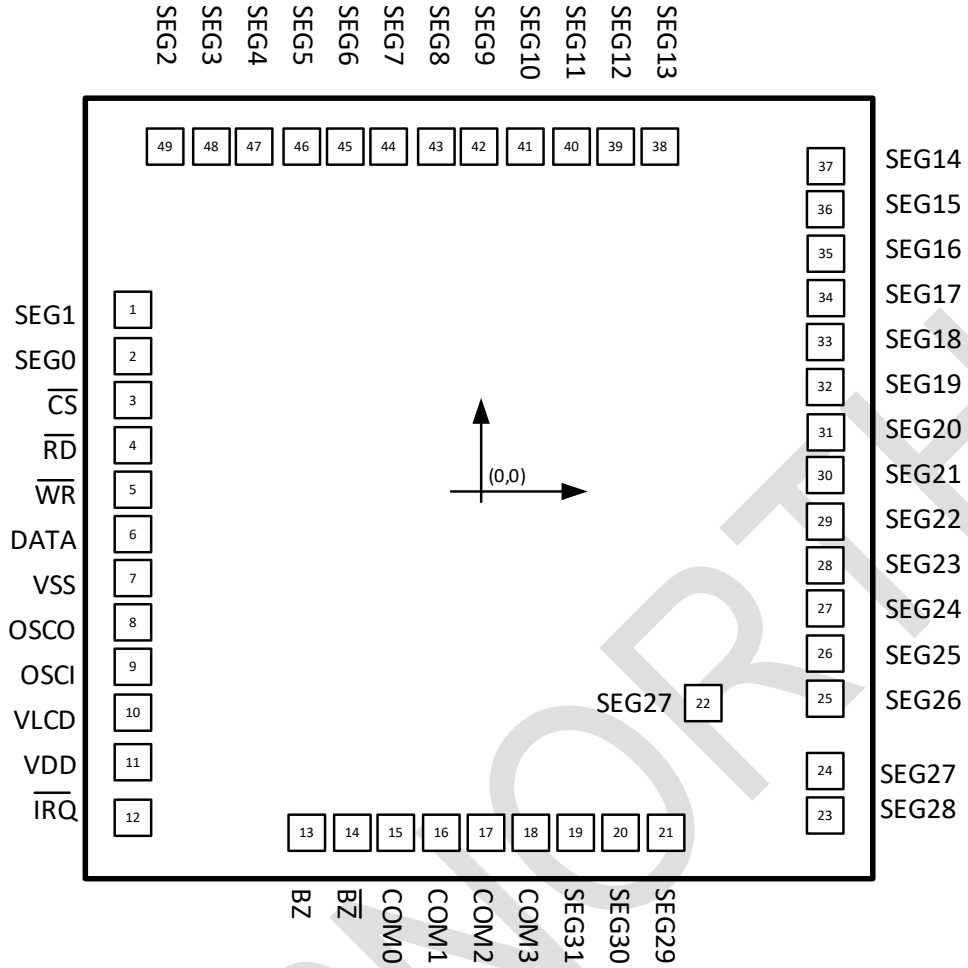






Note: The SEG27 and SEG28 is not in sequential order in the LQFP-48 package.

7 PAD Assignment for COB

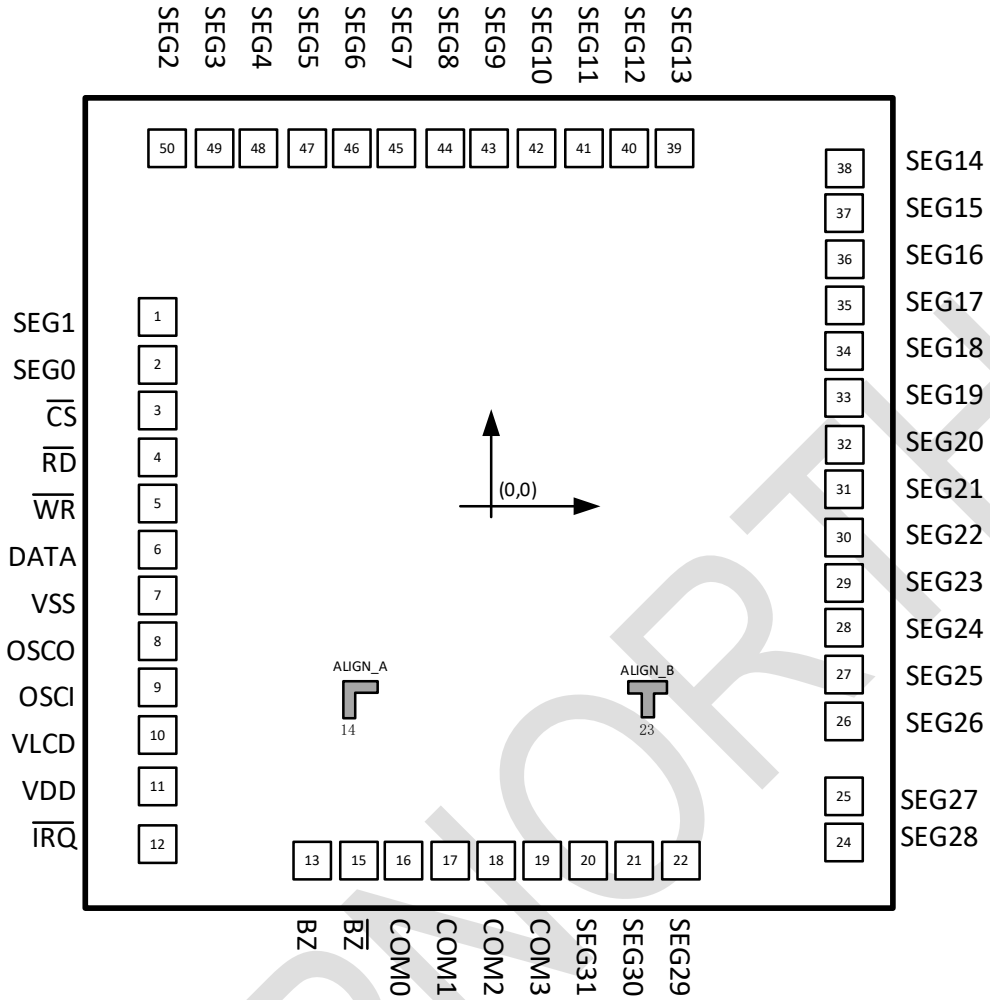


8 PAD Coordinates for COB

UNIT: μm

No	Name	X	Y	No	Name	X	Y
1	SEG1	-577.500	300.780	26	SEG25	577.500	-275.445
2	SEG0	-577.500	225.780	27	SEG24	577.500	-200.445
3	$\overline{CS}$	-577.500	150.780	28	SEG23	577.500	-125.445
4	$\overline{RD}$	-577.500	75.780	29	SEG22	577.500	-50.445
5	$\overline{WR}$	-577.500	0.780	30	SEG21	577.500	24.555
6	DATA	-577.500	-74.220	31	SEG20	577.500	99.555
7	VSS	-577.500	-149.220	32	SEG19	577.500	174.555
8	OSCO	-577.500	-224.220	33	SEG18	577.500	249.555
9	OSCI	-577.500	-299.220	34	SEG17	577.500	324.555
10	VLCD	-577.500	-374.220	35	SEG16	577.500	399.555
11	VDD	-577.500	-457.465	36	SEG15	577.500	474.555
12	$\overline{IRQ}$	-577.500	-553.370	37	SEG14	577.500	549.555
13	BZ	-288.990	-576.500	38	SEG13	301.020	576.500
14	$\overline{BZ}$	-213.990	-576.500	39	SEG12	226.020	576.500
15	COM0	-138.990	-576.500	40	SEG11	151.020	576.500
16	COM1	-63.990	-576.500	41	SEG10	76.020	576.500
17	COM2	11.010	-576.500	42	SEG9	1.020	576.500
18	COM3	86.010	-576.500	43	SEG8	-73.980	576.500
19	SEG31	161.010	-576.500	44	SEG7	-148.980	576.500
20	SEG30	236.010	-576.500	45	SEG6	-223.980	576.500
21	SEG29	311.010	-576.500	46	SEG5	-298.980	576.500
22	SEG27	374.110	-358.830	47	SEG4	-373.980	576.500
23	SEG28	577.500	-546.960	48	SEG3	-448.980	576.500
24	SEG27	577.500	-471.960	49	SEG2	-523.980	576.500
25	SEG26	577.500	-350.445				

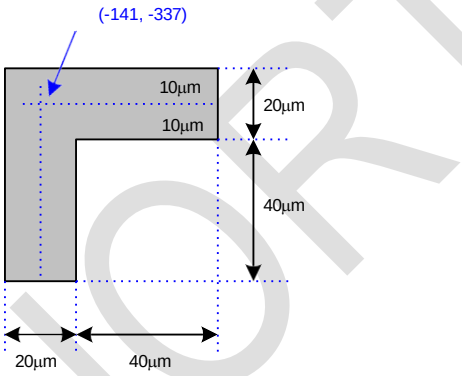
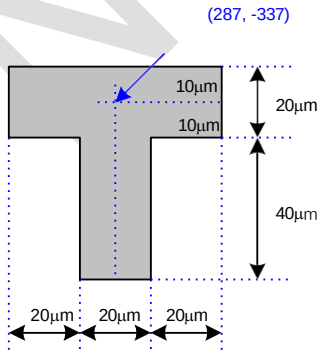
9 PAD Assignment for COG



10 PAD Dimensions for COG

Item	Pad Number	Size		Unit
		X	Y	
Chip size	—	1328	1326	μm
Chip thickness	—			μm
Pad pitch	All Pad	≥75		μm
Bump size	1~12, 24~38	54	44	μm
	13,15~22,39~50	44	54	μm
Bump Spacing	All pad	≥21		μm
Bump height	All pad	18±3		μm

11 Alignment Mark Dimensions for COG

Item	Number	Size	Unit
ALIGN_A	14		μm
ALIGN_B	23		μm

12 PAD Coordinates for COG

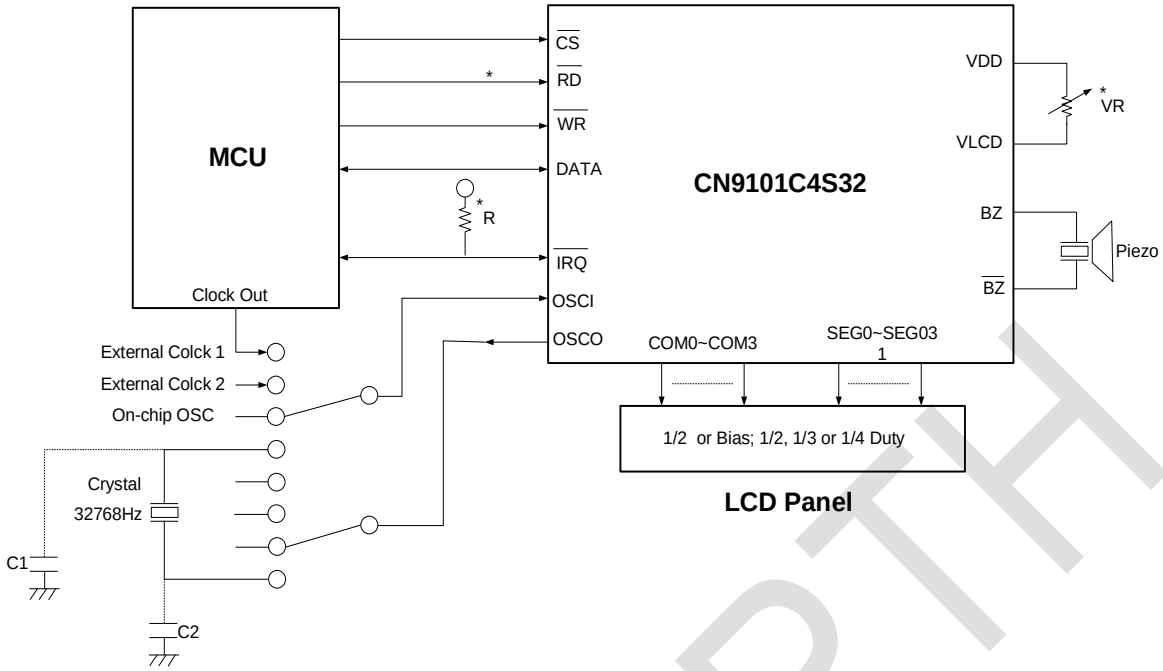
UNIT: μm

No	Name	X	Y	No	Name	X	Y
1	SEG1	-513.000	300.780	26	SEG26	575.000	-350.445
2	SEG0	-513.000	225.780	27	SEG25	575.000	-275.445
3	$\overline{CS}$	-513.000	150.780	28	SEG24	575.000	-200.445
4	$\overline{RD}$	-513.000	75.780	29	SEG23	575.000	-125.445
5	$\overline{WR}$	-513.000	0.780	30	SEG22	575.000	-50.445
6	DATA	-513.000	-74.220	31	SEG21	575.000	24.555
7	VSS	-513.000	-149.220	32	SEG20	575.000	99.555
8	OSCO	-513.000	-224.220	33	SEG19	575.000	174.555
9	OSCI	-513.000	-299.220	34	SEG18	575.000	249.555
10	VLCD	-513.000	-374.220	35	SEG17	575.000	324.555
11	VDD	-513.000	-457.465	36	SEG16	575.000	399.555
12	$\overline{IRQ}$	-513.000	-553.370	37	SEG15	575.000	474.555
13	BZ	-288.990	-574.000	38	SEG14	575.000	549.555
14	ALIGN_A	-141.000	-337.000	39	SEG13	301.020	574.000
15	$\overline{BZ}$	-213.990	-574.000	40	SEG12	226.020	574.000
16	COM0	-138.990	-574.000	41	SEG11	151.020	574.000
17	COM1	-63.990	-574.000	42	SEG10	76.020	574.000
18	COM2	11.010	-574.000	43	SEG9	1.020	574.000
19	COM3	86.010	-574.000	44	SEG8	-73.980	574.000
20	SEG31	161.010	-574.000	45	SEG7	-148.980	574.000
21	SEG30	236.010	-574.000	46	SEG6	-223.980	574.000
22	SEG29	311.010	-574.000	47	SEG5	-298.980	574.000
23	ALIGN_B	287.000	-337.000	48	SEG4	-373.980	574.000
24	SEG28	575.000	-546.960	49	SEG3	-448.980	574.000
25	SEG27	575.000	-471.960	50	SEG2	-523.980	574.000

13 PAD Descriptions

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection signal input with pull-high resistor, active low If $\overline{CS}$ is high, the serial interface circuit is reset, and data and commands of CN9101C4S32 are invalid. If $\overline{CS}$ is low, the primary controller can read and write CN9101C4S32 data.
2	$\overline{RD}$	I	Read clock input with pull-high resistor At the falling edge of the $\overline{RD}$ signal, CN9101C4S32 outputs DATA to the data line. The host controller can latch this output data at the next rising edge.
3	$\overline{WR}$	I	Write clock input with pull-high resistor Data on the DATA line are latched into the CN9101C4S32 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor.
5	VSS	-	Negative power supply, ground.
6	OSCI	I	When using a crystal oscillator as a system clock source, a 32.768kHz crystal oscillator can be connected between the OSCI and OSCO pads. If the external clock input is used as the system clock source, the external clock source connects to the OSCI pin. Using the internal RC oscillator, OSCI and OSCO pins float empty.
7	OSCO	O	
8	VLCD	I	LCD power input.
9	VDD	-	Positive power supply.
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output.
11,12	BZ,$\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair.
13~16	COM0~COM3	O	LCD common outputs.
48~17	SEG0~SEG31	O	LCD segment outputs.

14 Typical Application



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

The voltage applied to VLCD pin must be equal to or lower than VDD.

Adjust VR to fit user's LCD panel display voltage (VLCD)

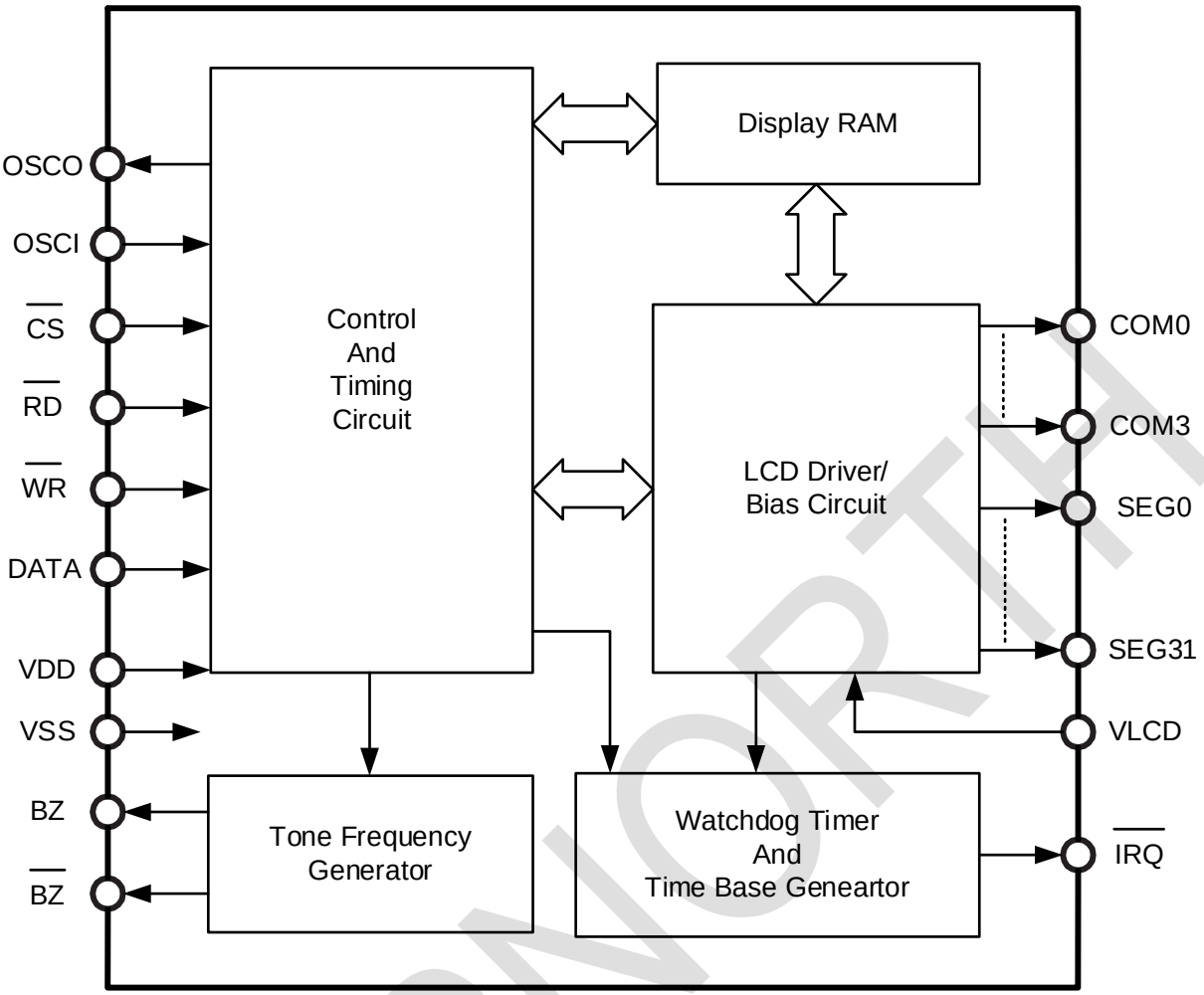
Adjust R (external pull-high resistance) to fit user's time base clock.

In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which. suggests the value of capacities

The table illustrates the suggestion value of capacities (C1,C2)

Crystal Error	Capacity Value
±10ppm	0~10pF
10~20ppm	10~20pF

15 Block Diagram



16 Specifications

16.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	VSS-0.3 to VSS+6.5	V
Input Voltage	V_{IN}	VSS-0.3 to VDD+0.3	V
Storage Temperature	T_{stg}	-55 to +150	℃
Operating Temperature	T_{opr}	-40 to +105	℃

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

17 D.C. Characteristics

Ta= 25°C

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VDD	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	7.9	15.8	μA
		5V		—	9.4	18.8	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	8.7	17.4	μA
		5V		—	15.8	31.6	μA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	6.6	13.2	μA
		5V		—	8.7	17.4	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	0.1	1.0	μA
		5V		—	0.3	2.0	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	—	—	0.6	V
		5V		—	—	0.8	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	1.6	—	—	V
		5V		2.0	—	—	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	VOL=0.3V	6	8.8	—	mA
		5V	VOL=0.5V	12	19.9	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	VOH=2.7V	-6	−8.1	—	mA
		5V	VOH=4.5V	-12	−17.5	—	mA
I_{OL2}	LCD Common Sink Current	3V	VOL=0.3V	250	451	—	μA
		5V	VOL=0.5V	500	792	—	μA
I_{OH2}	LCD Common Source Current	3V	VOH=2.7V	-140	−229	—	μA
		5V	VOH=4.5V	-200	−388	—	μA
I_{OL3}	LCD Segment Sink Current	3V	VOL=0.3V	250	466	—	μA
		5V	VOL=0.5V	500	783	—	μA
I_{OH3}	LCD Segment Source Current	3V	VOH=2.7V	-140	−223	—	μA
		5V	VOH=4.5V	-300	−389	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	—	200	—	kΩ
		5V		—	100	—	kΩ

18 A.C. Characteristics

Ta= 25°C

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VDD	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	28.8	32.0	35.2	kHz
f_{SYS2}	System Clock	—	Crystal oscillator	—	32768	—	Hz
f_{SYS3}	System Clock	—	External clock source	—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	f_{SYS1}/128	—	Hz
		—	Crystal oscillator	—	f_{SYS2}/128	—	Hz
		—	External clock source	—	f_{SYS3}/1024	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	—	—	1000	kHz
		5V		—	—	2000	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	500	kHz
		5V		—	—	1000	kHz
f_{TONE}	Tone Frequency (2kHz)	3V	On-chip RC oscillator	1.5	2.0	2.5	kHz
	Tone Frequency (4kHz)	5V		3.0	4.0	5.0	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	250	300	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	0.50	—	—	μs
			Read mode	1.00	—	—	
		5V	Write mode	0.25	—	—	μs
			Read mode	0.50	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	C_O=15pF	—	50	100	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	50	100	—	ns
t_h	Hold DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	100	200	—	ns
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	200	300	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	100	200	—	ns
t_{PD}	DATA Output Delay Time ($\overline{RD}$ Falling to DATA)	—	C_O=15pF t_{PD}=50% to 50%	—	100	200	ns
t_{OFF}	VDD OFF Times (Figure 4)	—	VDD drop down to 0V	20	—	—	ms
t_{SR}	VDD Rising Slew Rate (Figure 4)	—		0.05	—	—	V/ms
t_{RSTD}	Delay Time after Reset (Figure 4)	—		1	—	—	ms

Note: If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

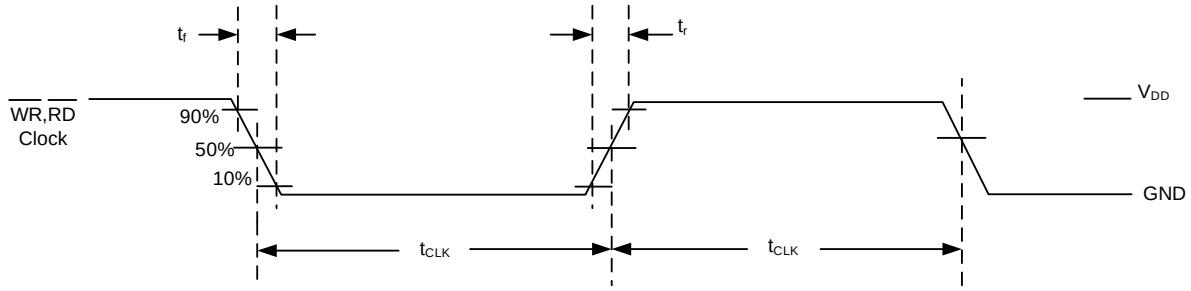


Figure1

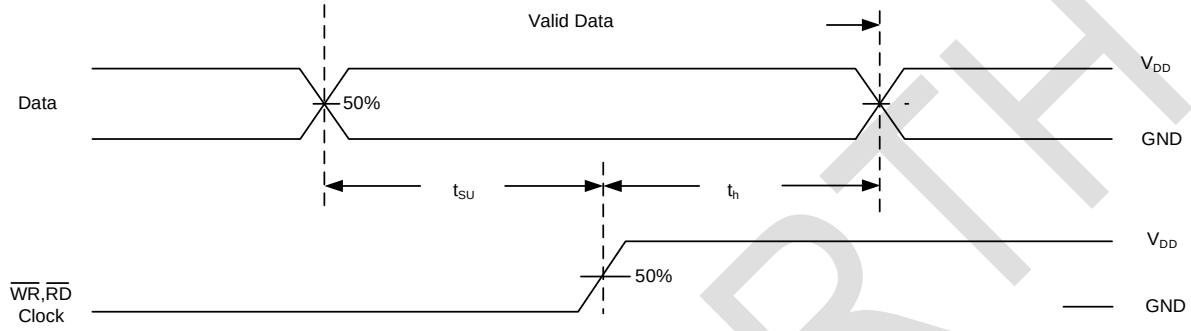


Figure2

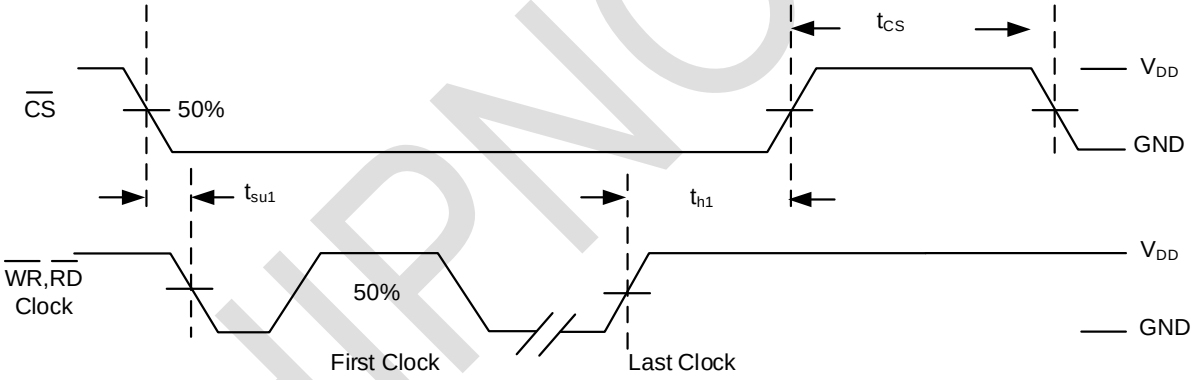


Figure3

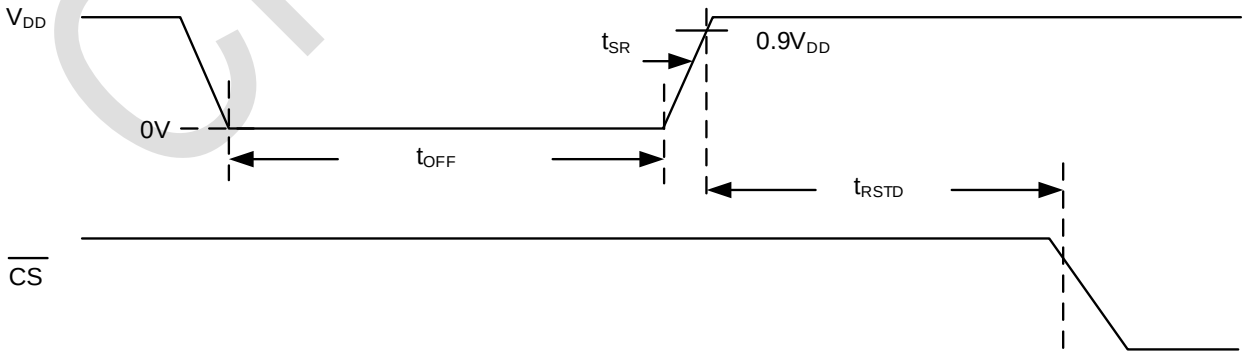


Figure4

19 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	100	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	100	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	100	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-X000-X	C	Time base/WDT clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output: 4Hz The WDT time-out flag after: 1s	

F8	100	101X-X011-X	C	Time base/WDT clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode, user don't use.	
NORMAL	100	1110-0011-X	C	Normal mode	

Note: X: Don't care

A5~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

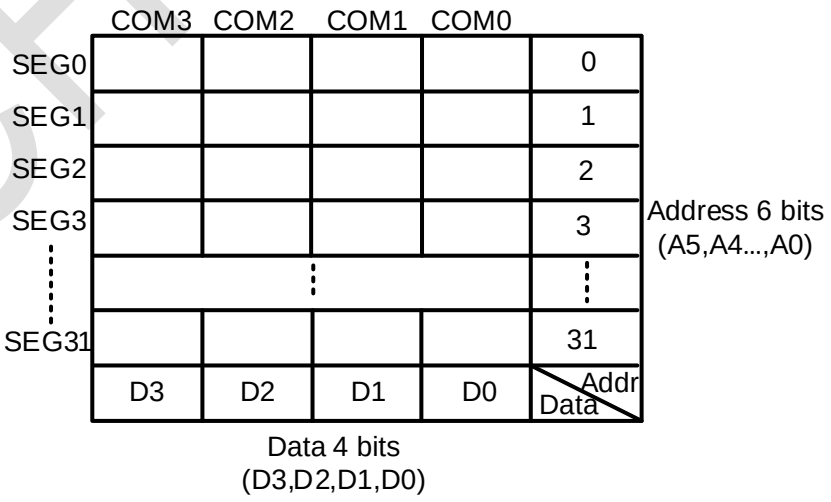
Def.: Power on reset default

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Of these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the CN9101C4S32 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the CN9101C4S32.

20 Functional Description

20.1 Display Memory - RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



20.2 System Oscillator

The CN9101C4S32 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency.

System clock source Through software configuration, you can choose RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the software setting. The configuration of the system oscillator is as shown.

After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. However, this command only works with internal RC oscillators and crystal oscillators. Once the system clock is stopped, the LCD display is turned off and the time base /WDT function stops working.

The LCD OFF command is used to disable the LCD bias generator. You can run the SYS DIS command after the LCD OFF command to enter the power saving mode. However, if the system clock is from an external clock source, the SYS DIS command cannot disable the system clock and therefore cannot enter the power saving mode.

After the power-on, the initial status of the system clock is SYS DIS.

20.3 Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc.

The WDT time-out will result in the setting of an internal WDT time out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

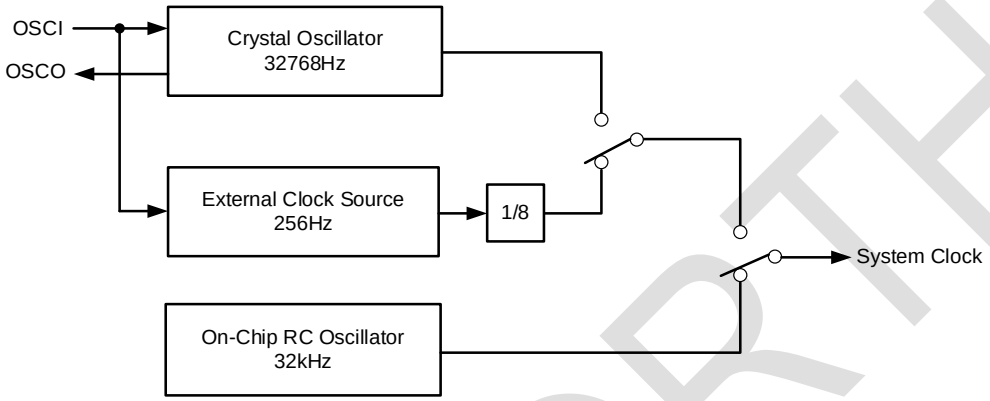
$$f_{WDT} = \frac{32kHz}{2^n}$$

Where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (32kHz), or an external frequency of 256kHz.

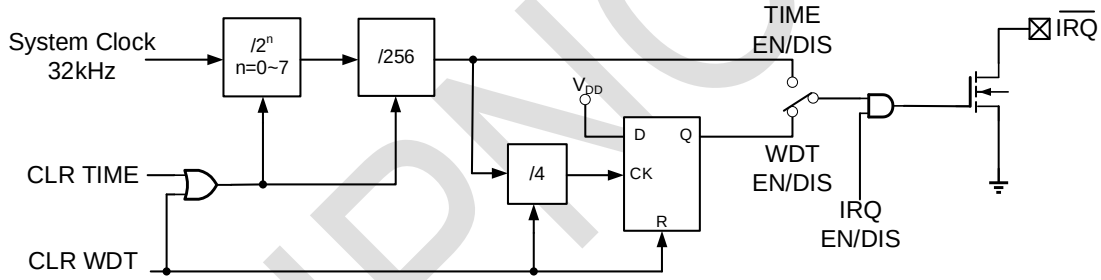
If an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN

or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time- out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the CN9101C4S32 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.



System Oscillator Configuration



Timer and WDT Configurations

20.4 Tone Output

A simple tone generator is implemented in the CN9101C4S32. a pair of differential drive signals are generated and output via BZ and $\overline{BZ}$ to drive a single tone for a voltage-type buzzer.

The TONE generator can produce TONE outputs at two frequencies, 4kHz or 2kHz, which can be selected by software configuration TONE 4k or TONE 2k commands. When the system clock is turned off or the TONE output is turned off, BZ and $\overline{BZ}$ remain low.

20.5 LCD Driver

The CN9101C4S32 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the software configuration. This feature makes the CN9101C4S32 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted.

LCD ON turns on the LCD bias generator, and LCD OFF turns off the LCD bias generator. BIAS and COM configure commands related to LCD display, and by using this instruction, CN9101C4S32 can be compatible with most types of LCD panels.

Name	Command Code	Function
LCD OFF	**1 0 0** 0 0 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	**1 0 0** 0 0 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	**1 0 0** 0 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

20.6 Command Format

The CN9101C4S32 can be configured by the software setting. There are two mode commands to configure the CN9101C4S32 resources and to transfer the LCD display data. The configuration mode of the CN9101C4S32 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID.

The mode command needs to be issued prior to the transfer of data or commands. If successive commands have been issued, the command mode ID 1 0 0 can be omitted. While the system is operating in the non-successive command or non-successive address data mode, the $\overline{CS}$ pin should be set to "1", and the previous operation mode will be reset. Once the $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

20.7 Interfacing

Only four lines are required to interface with the CN9101C4S32.

The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the CN9101C4S32. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the CN9101C4S32 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the CN9101C4S32.The DATA line is the serial data input/output line.

The Data to be read or written or commands to be written have to be passed through the DATA line.

The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal.

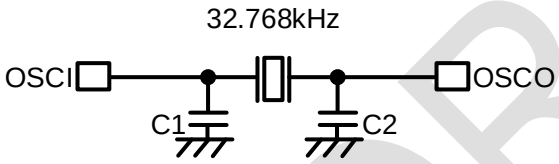
The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the CN9101C4S32 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the CN9101C4S32.

The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the CN9101C4S32.

20.8 Crystal Selection

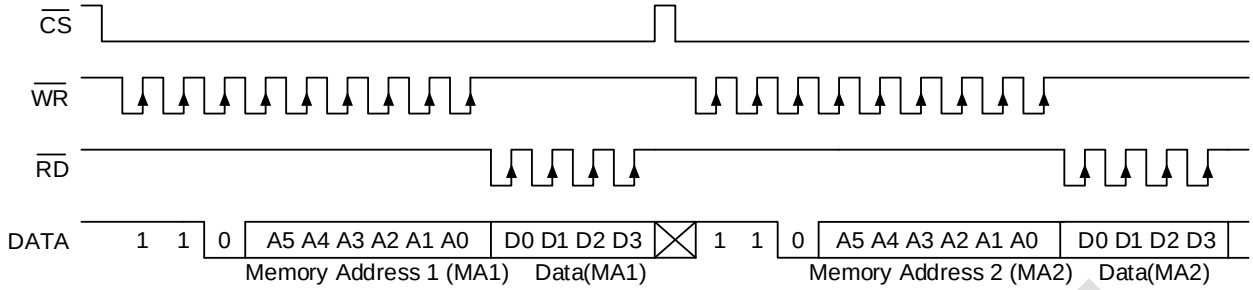
A 32.768kHz crystal can be directly connected to the CN9101C4S32 via OSCI and OSCO. In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities. The table illustrates the suggestion value of capacities (C1, C2).

Crystal Error	Capacity Value
±10ppm	0~10pF
10~20ppm	10~20pF

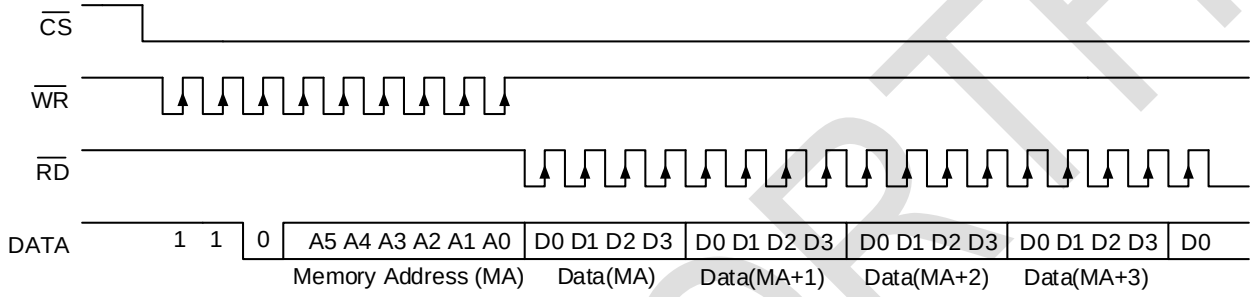


20.9 Timing Diagrams

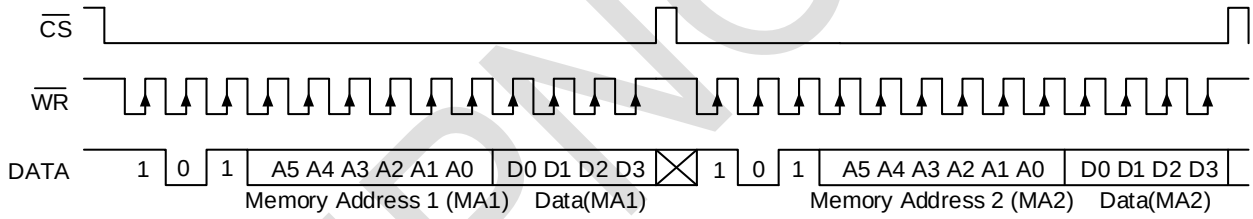
20.9.1 READ Mode (Command Code :110)



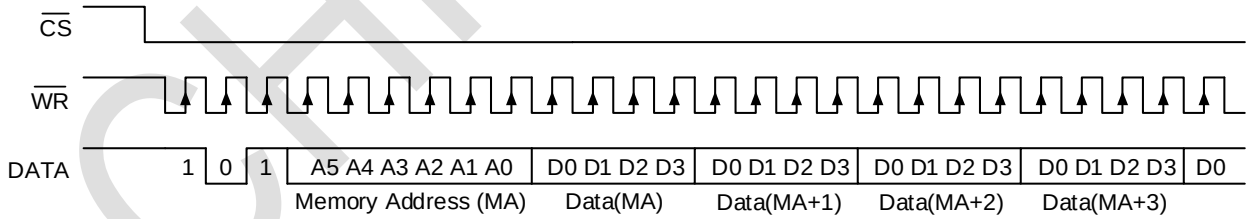
20.9.2 READ Mode (Successive Address Reading)



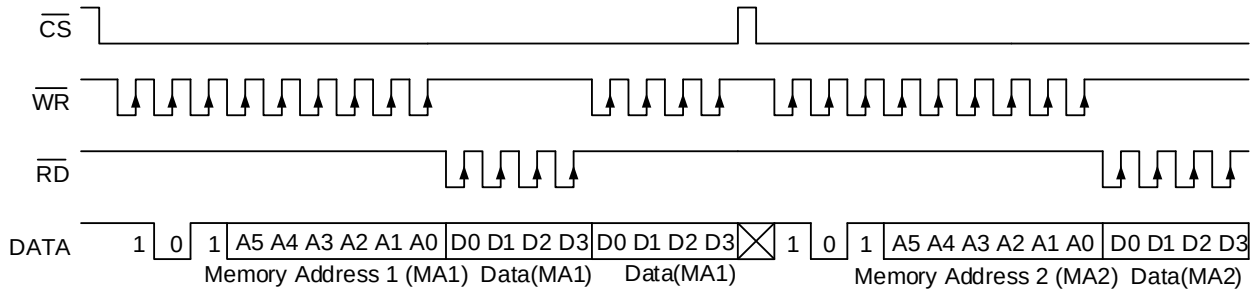
20.9.3 WRITE Mode (Command Code:101)



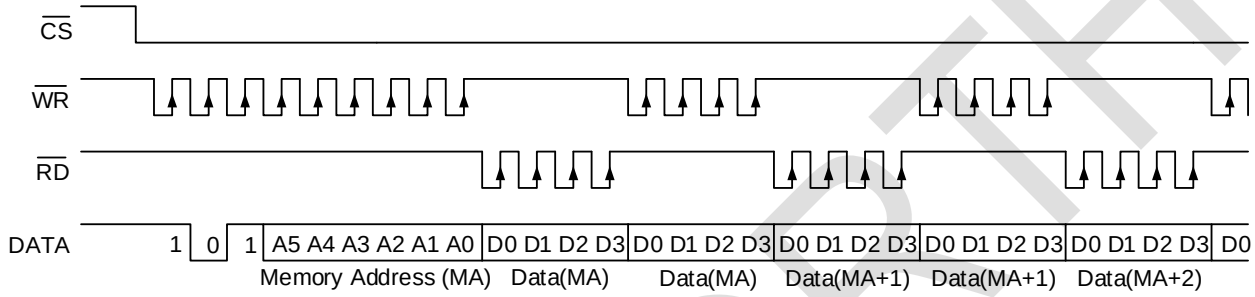
20.9.4 WRITE Mode (Successive Address Writing)



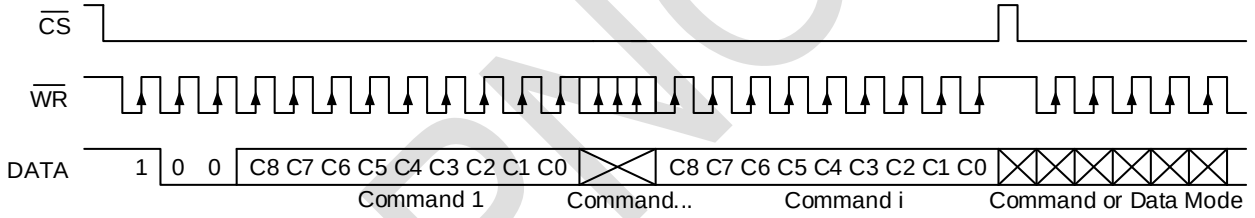
20.9.5 Read-Modify-Write Mode (Command Code :101)



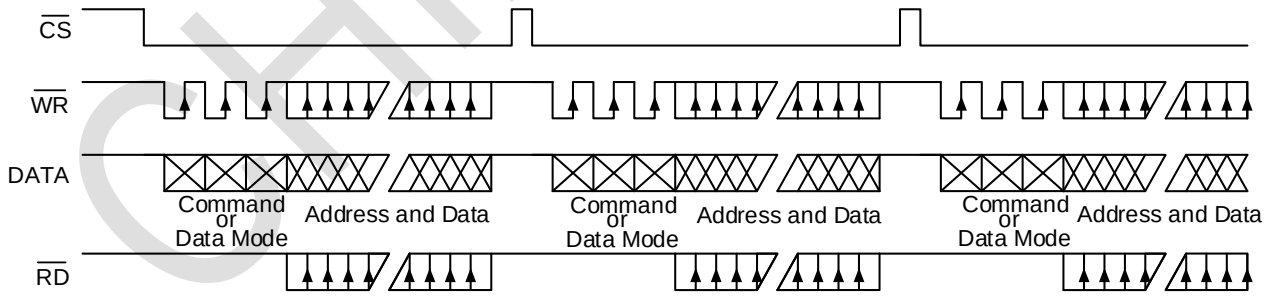
20.9.6 Read-Modify-Write Mode (Successive Address Reading)



20.9.7 Command Mode (Command Code :100)

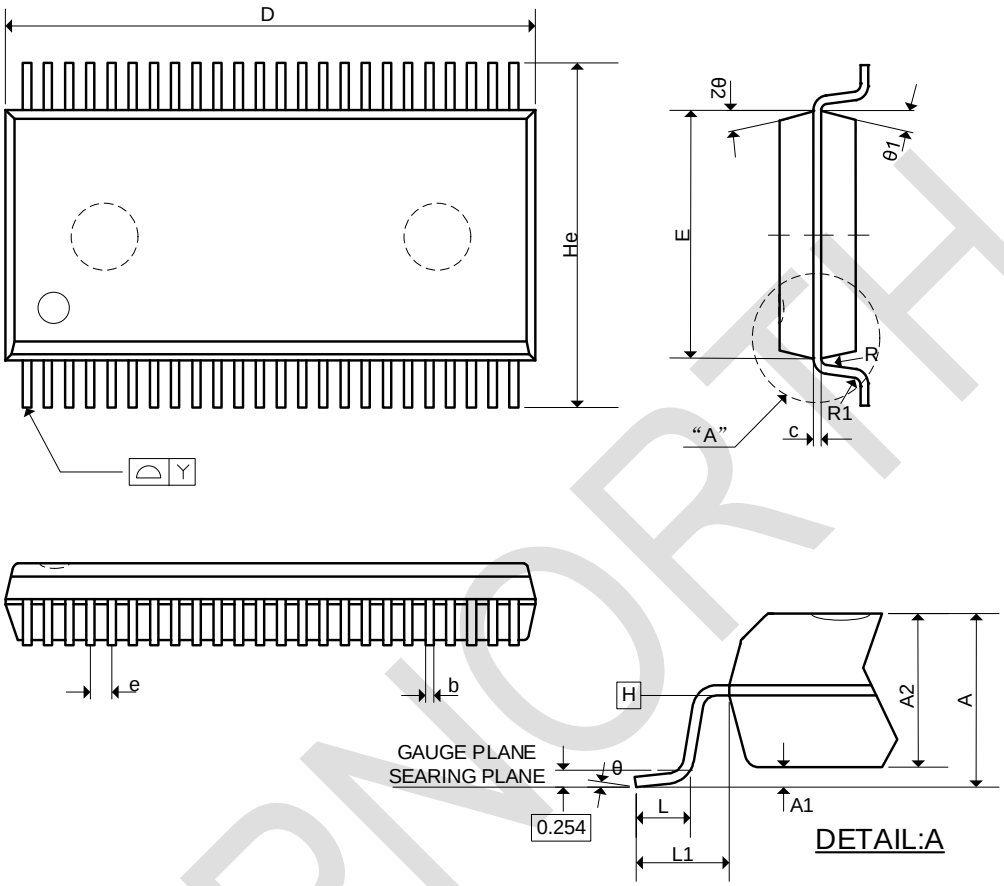


20.9.8 Mode (Data and Command Mode)



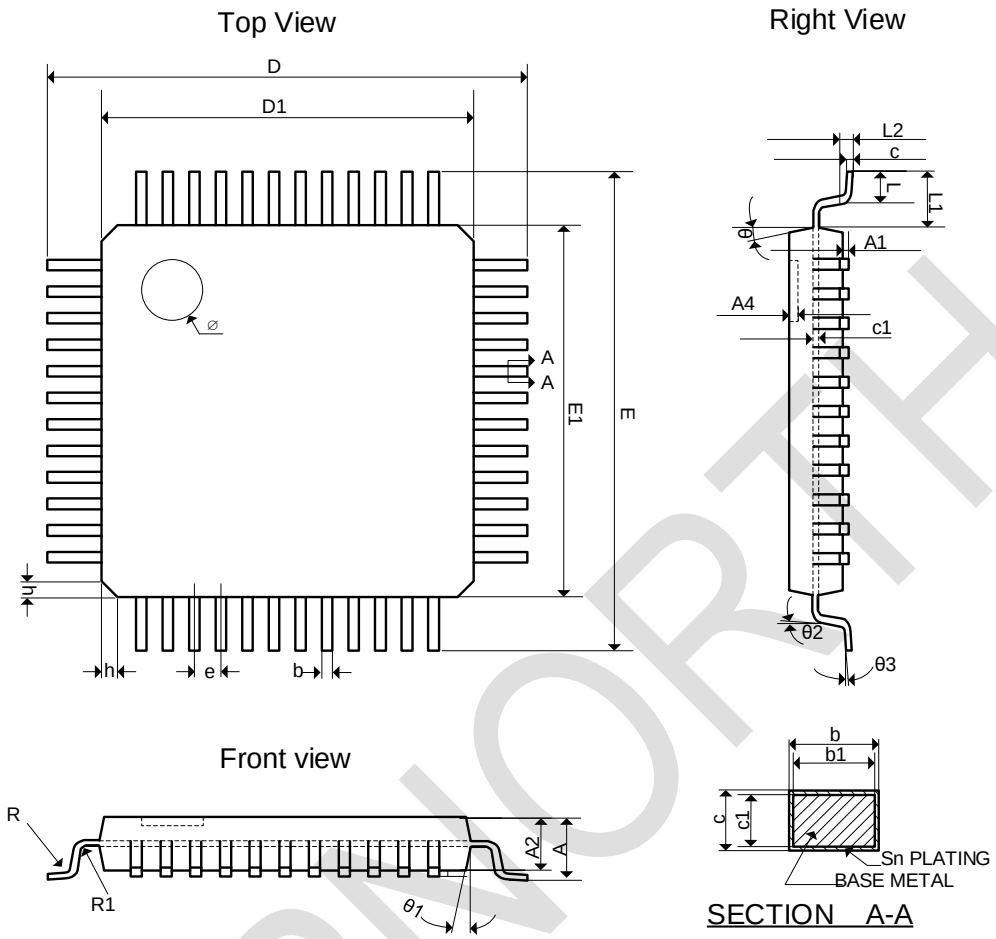
21 Package Information

SSOP48



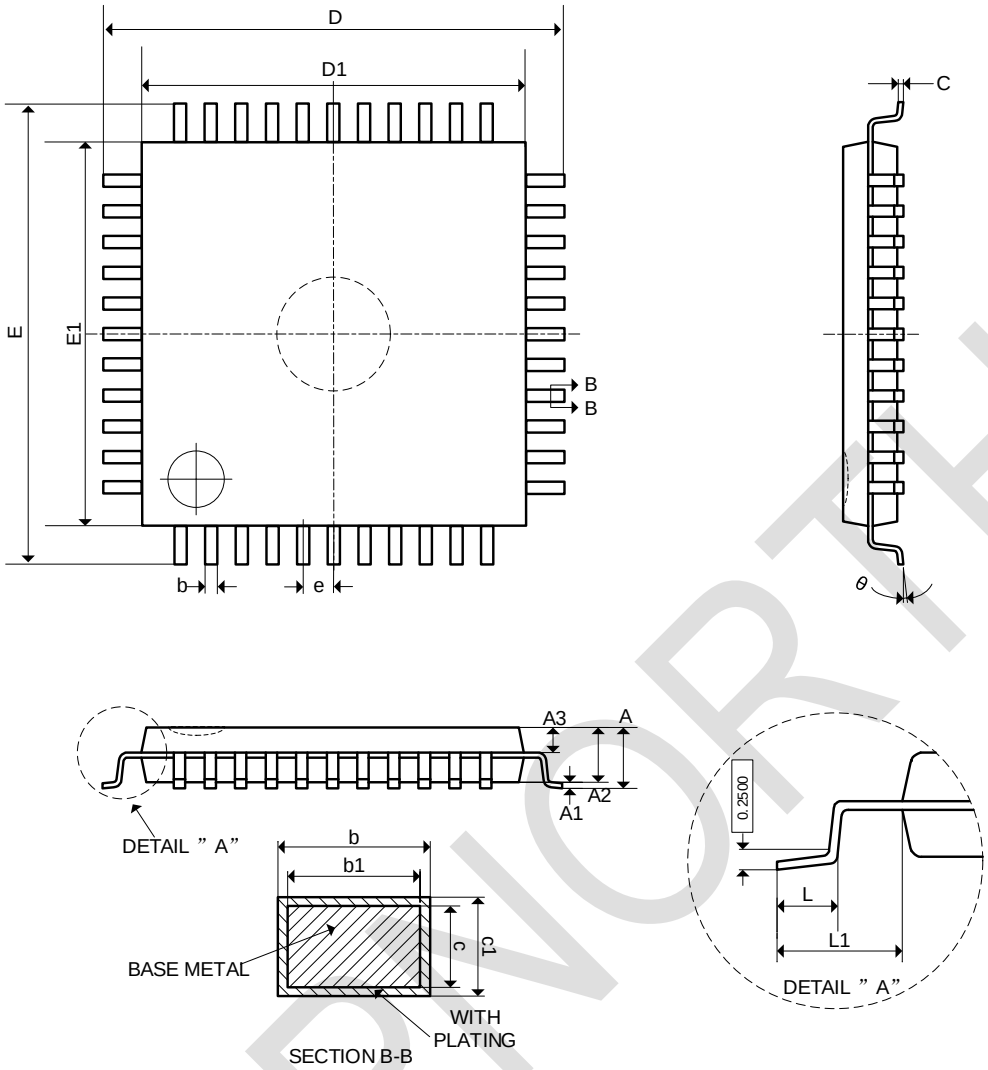
SIZE / SYMBOL	MIN (mm)	MON (mm)	MAX (mm)	SIZE / SYMBOL	MIN (mm)	MON (mm)	MAX (mm)
A	2.413	2.500	2.794	L	0.570	0.700	0.954
A1	0.103	0.200	0.306	L1	-	1.400	-
A2	2.159	2.300	2.413	Y	-	-	0.076
b	0.203	0.254	0.330	θ	0°	-	8°
c	-	0.152	-	θ1	-	15°TYPE	-
D	15.698	15.850	16.002	θ2	-	15°TYPE	-
E	7.391	7.500	7.595	R	-	0.20 TYPE	-
e	-	0.635	-	R1	-	0.25 TYPE	-
He	10.058	10.300	10.566				

LQFP48



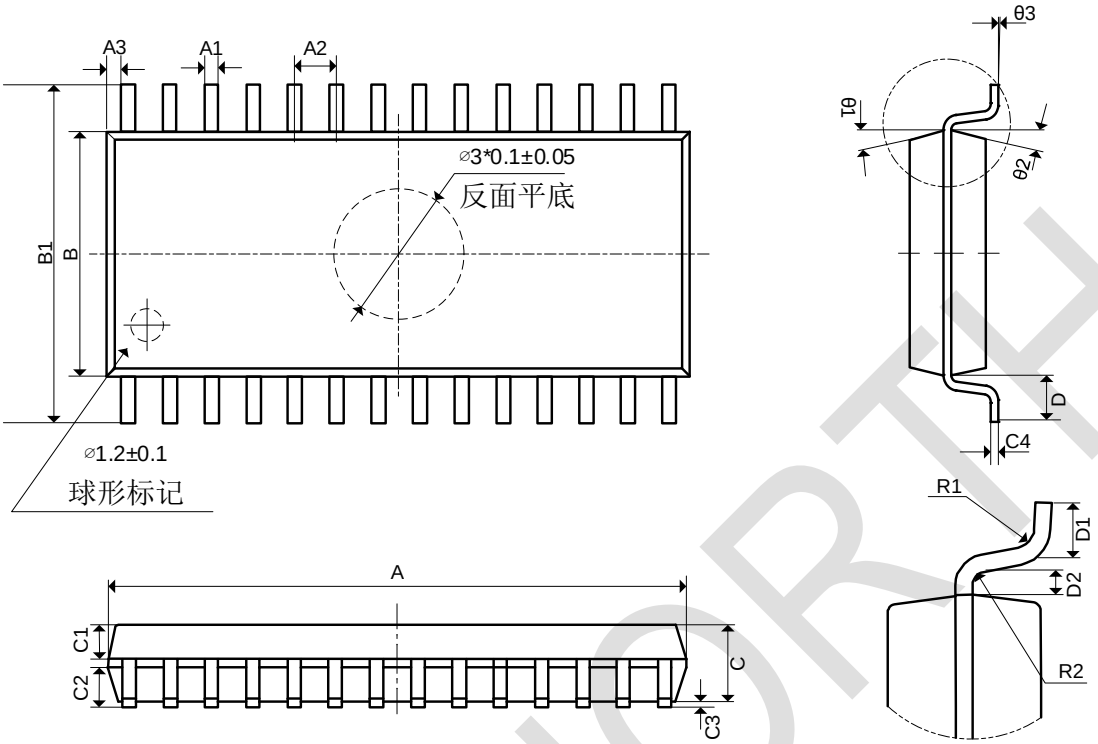
	SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)		SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)
TOTAL THICKNESS	A	-	-	1.60	LEAD PITCH	e	0.50BSC		
STAND OFF	A1	0.05	0.10	0.20	CHAMFER	h	0.20	0.30	0.40
BODY THICKNESS	A2	1.35	1.40	1.45	FOOT LENGTH	L	0.45	0.65	0.75
UP BODY THICKNESS	A3	0.64BSC			LEAD LENGTH	L1	1.00BSC		
THIMBLE DEPTH	A4	0.10	0.20	0.30	MEASURE POINT	L2	0.25BSC		
LEAD WIDTH	b	0.17	0.225	0.28	R RADIUS	R	0.15 REF		
LEAD WIDTH	b1	0.20BSC			R1 RADIUS	R1	0.12 REF		
L/F THICKNESS	c	0.127	-	0.16	ANGLE FOR MOLD	θ	12° TYP		
L/F THICKNESS	c1	0.107	0.127	0.147	ANGLE FOR MOLD	θ1	12° TYP		
TOTAL SIZE X	D	8.80	9.00	9.20	ANGLE FOR LEAD	θ2	4° TYP		
BODY SIZE X	D1	6.90	7.00	7.10	ANGLE FOR FOOT	θ3	0° ~8°		
TOTAL SIZE Y	E	8.80	9.00	9.20	THIMBLE DIAMETER	Ø	1.10	1.20	1.30
BODY SIZE Y	E1	6.90	7.00	7.10					

LQFP44



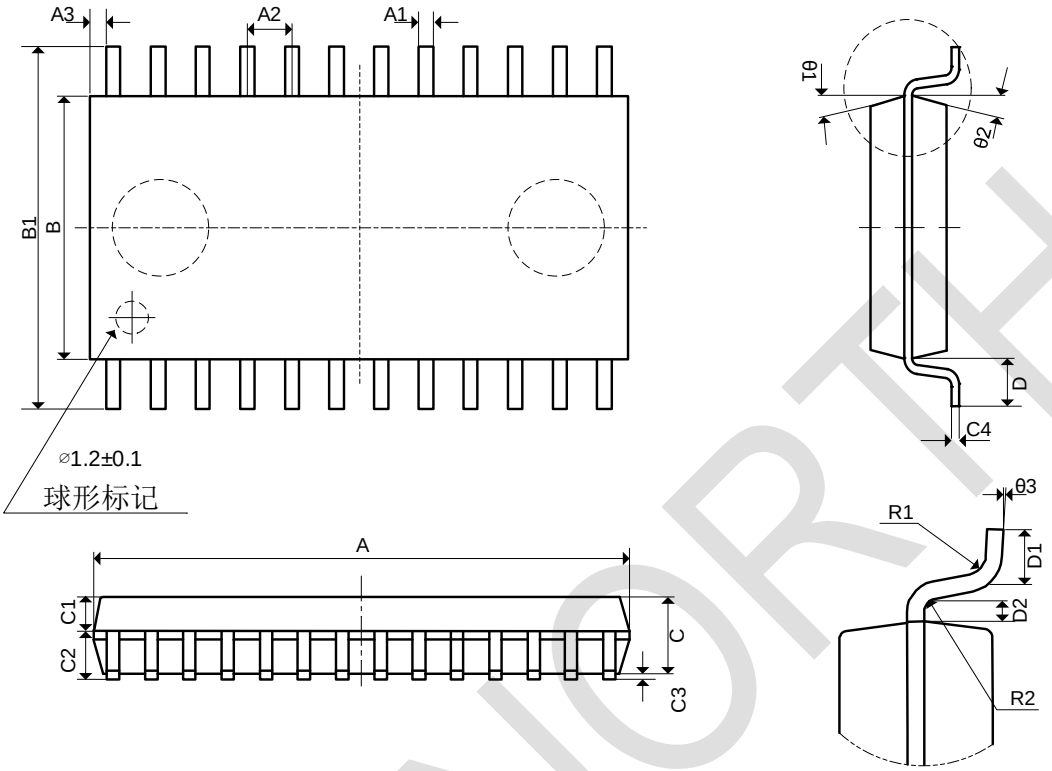
SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)		SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)
TOTAL THICKNESS	A	-	-	1.60	LEAD SPAN(X)	D	11.80	12.00	12.20
STAND OFF	A1	0.05	0.10	0.15	MOLD LENGTH(X)	D1	9.90	10.00	10.10
MOLD TOTAL THICKNESS	A2	1.35	1.40	1.45	LEAD SPAN(Y)	E	11.80	12.00	12.20
TOP MOLD THICKNESS	A3	0.59	0.64	0.69	MOLD WIDTH(Y)	E1	9.90	10.00	10.10
LEAD WIDTH	b	0.28	-	0.36	LEAD PITCH	e	0.80BSC		
LEAD WIDTH	b1	0.27	0.30	0.33	LEAD SOLE LENGTH	L	0.45	0.60	0.75
LEAD THICKNESS	c	0.13	-	0.17	LEAD LENGTH	L1	1.0REF		
LEAD THICKNESS	c1	0.12	0.13	0.14	LEAD FORM ANGLE	θ	0°	-	7°

SOP28



SIZE / SYMBOL	MIN (mm)	MAX (mm)	SIZE / SYMBOL	MIN (mm)	MAX (mm)
A	17.90	18.10	C4	0.244	0.264
A1	0.356	0.456	D	1.353	1.453
A2	1.17	1.37	D1	0.60	1.00
A3	0.542TYP		D2	0.18TYP	
B	7.40	7.60	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.18	2.28	θ1	12° TYP4	
C1	0.938	1.038	θ2	12° TYP4	
C2	0.938	1.038	θ3	0° ~8°	
C3	0.03	0.17			

SOP24



SIZE / SYMBOL	MIN (mm)	MAX (mm)	SIZE / SYMBOL	MIN (mm)	MAX (mm)
A	15.19	15.39	C4	0.246	0.262
A1	0.406TYP		D	1.34	1.44
A2	1.22	1.32	D1	1.21TYP	
A3	0.457TYP		D2	0.18TYP	
B	7.40	7.60	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.13	2.33	θ1	12°TYP4	
C1	0.938	1.038	θ2	12°TYP4	
C2	1.192	1.292	θ3	0°~8°	
C3	0.145	0.205			

22 Important Statement

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