24V/800mA Synchronous Buck Converter

1 Description

The CN2203TER is a 3.8V-24V wide input voltage range synchronous buck converter with 30V input over-voltage protection, capable of driving a 0.8A load. The internal integration of two low R_{DSON} power MOS reduces conduction loss and improves efficiency. The chip adopts peak current mode control, which can achieve excellent dynamic performance and also makes the peripheral compensation circuit simple. Since the switching frequency is fixed at 600K, small size inductors and capacitors can be selected, as well as small size SOT23-6L package, which can realize small size power supply solution. With 15uA quiescent operating current and 2uA shutdown current, the CN2203TER is suitable for power supply systems with low power consumption requirements. The CN2203TER features cycle-by-cycle current limit hiccup OCP protection, input OVP, and thermal shutdown.

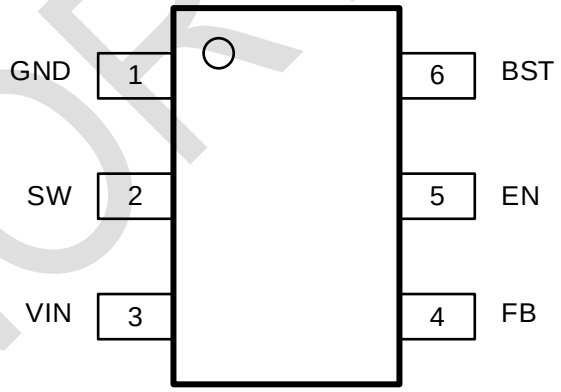
2 Features

- 3.8 V - 24 V wide input voltage range
- 30 V input overvoltage protection
- 0.8 A continuous output current
- 93% efficiency
- Low quiescent current of 15 μA
- 800 mV ±2% feedback reference voltage
- 600 kHz fixed switching frequency
- Light load PFM energy saving mode
- Frequency foldback function for 99% maximum duty cycle
- Internal ramp compensation to simplify external compensation circuitry
- Cycle-by-cycle peak and valley current limiting,more reliable overcurrent protection
- Hiccup mode overcurrent protection and short circuit protection
- FB short-circuit protection, which can effectively protect the back-end circuits
- 1 ms internal soft start to limit input inrush current
- Thermal shutdown

3 Applications

- Smart Meters
- Industrial applications
- Automotive applications
- Set-top boxes, routers, laptops, network terminals, memories

4 Pinout



SOT23-6L

5 Marking

Product Number	Marking
CN2203TER	CN2203 YYWW

Note: YY=Year WW=Week.

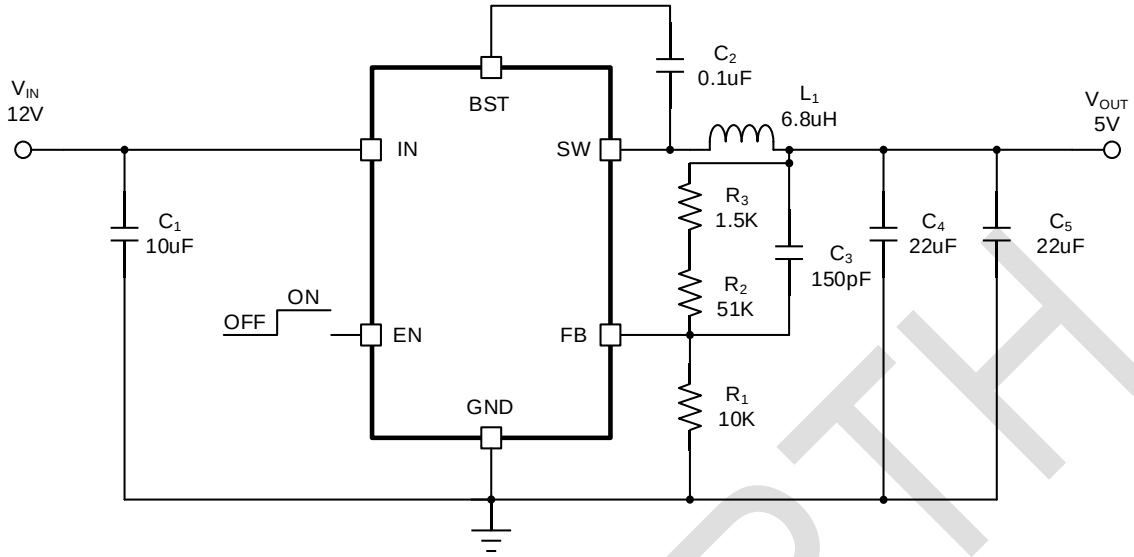
Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

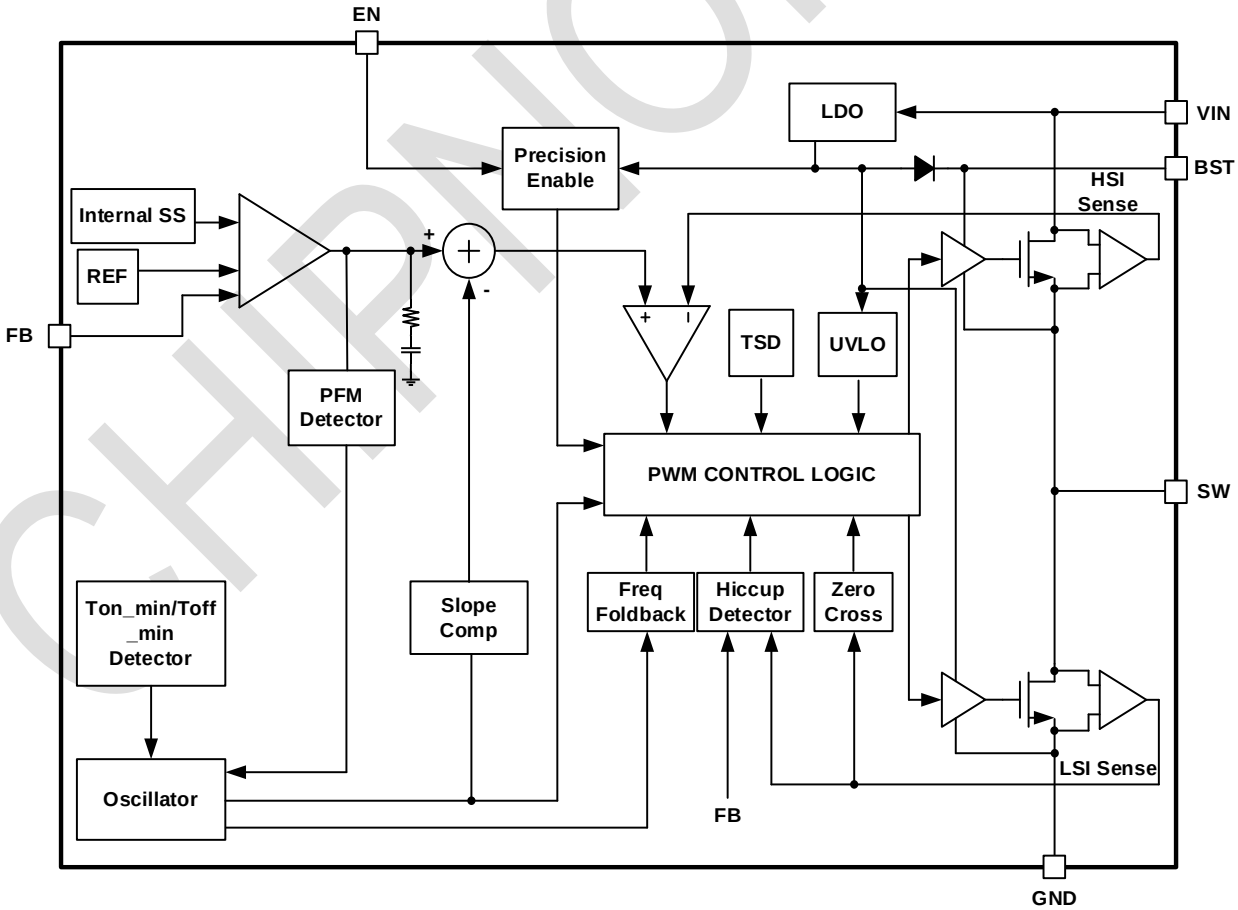
6 Ordering information

Product Number	Package	Quantity/Tape
CN2203TER	SOT23-6L	3000/Tape

7 Typical Application



8 Block Diagram



9 Pin Descriptions

Pin No.	Pin Name	Descriptions
6	BST	Bootstrap pin with 100 nF capacitor connected between BST-SW
1	GND	GND
4	FB	Feedback pin, connected to the middle node of a partial voltage resistor outside VOUT
5	EN	Enable pin, high level active, drive the pin to a high level to enable the chip, low level to disable the chip, normal high can connect EN to VIN
3	VIN	For power input, place a 10uF capacitor between VIN-GND and as close to the chip as possible
2	SW	Switch pin, connect an inductor between SW and VOUT

10 Specifications

10.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	-0.3 ~ 35	V
EN Operating Voltage	V_{SW}, V_{EN}	-0.3 ~ 36	V
SW Operating Voltag		-0.3 ~ VIN+0.3	
BST pin voltage	V_{BST}	-0.3 ~ VSW+6	V
FB pin voltage	V_{FB}	-0.3 ~ 6	V
Operating Junction Temperature Range	T_J	-40 ~ 150	°C
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Soldering Temperature	T_{LEAD}	260（soldering,10s）	°C
Storage Temperature Range	T_{STG}	-55 ~ 150	°C

NOTE: Operation beyond the absolute maximum ratings may cause damage to the device. Absolute maximum ratings do not indicate that the device will operate properly under these conditions or any other conditions other than the recommended operating conditions. If used outside of the recommended operating conditions but within the absolute maximum ratings, the device may not operate at full functionality, which may affect reliability, functionality, and performance and shorten device life.

10.2 ESD Ratings

Discharge mode	Value	Units
HBM	±4000	V
CDM	±2000	V
Latch up	±800	mA

10.3 Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units
Input Voltage Range	V_{IN}	3.8	24	V
Input Capacitance Range	C_{IN}	10		μF
Output Capacitance Range	C_{OUT}	22	100	μF
Bootstrap Capacitance Range	C_{BST}	100		nF
Inductance range	L	6.8		μH

10.4 Thermal Information

Parameter	Descriptions	Value	Unit
Junction to Ambient Thermal Resistance	$R\theta_{JA}$	173	°C/W
Thermal Resistance to Enclosure (Top)	$R\theta_{JC(top)}$	116	°C/W
Thermal Resistance to Circuit Board	$R\theta_{JB}$	31	°C/W

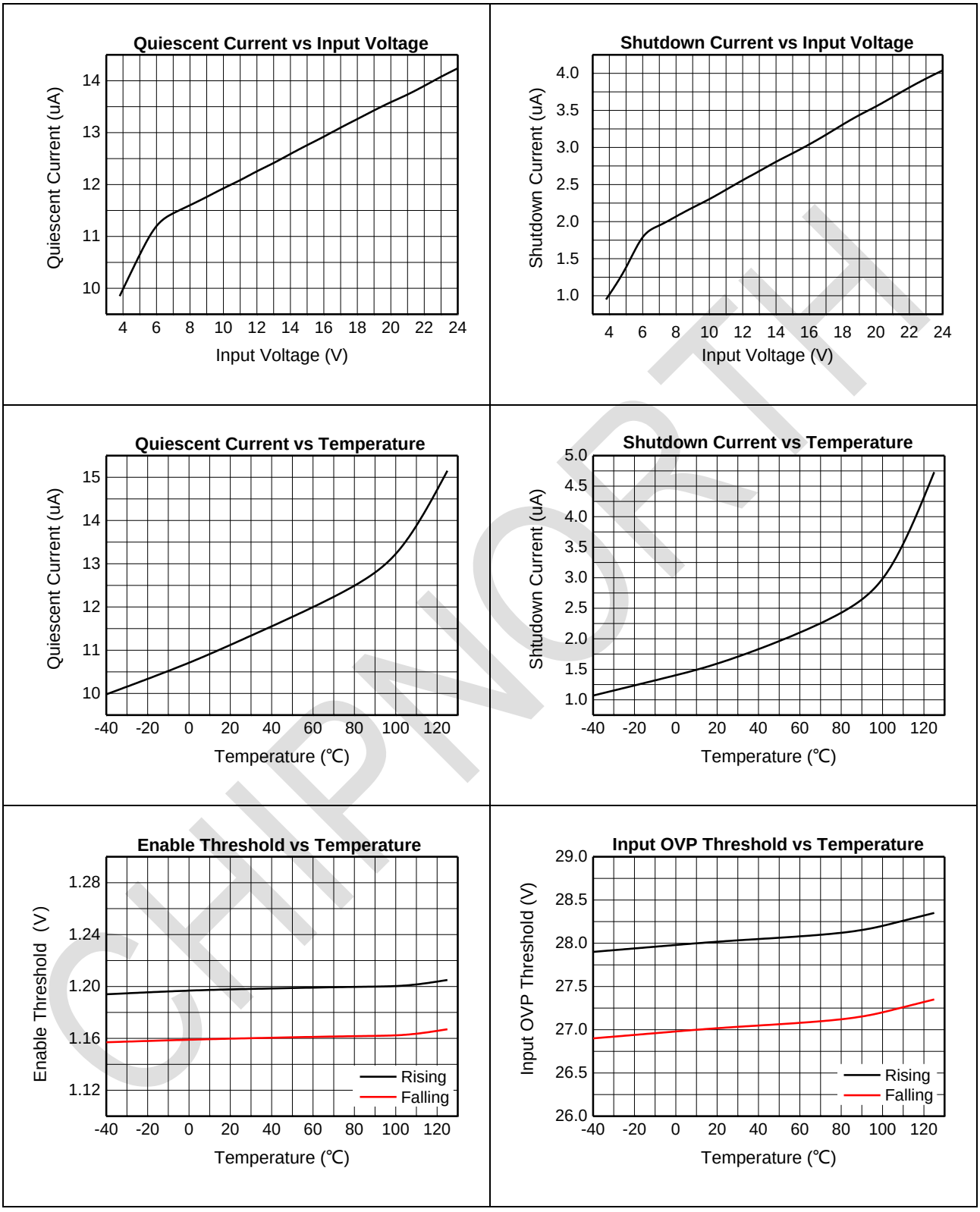
10.5 Electrical Characteristics

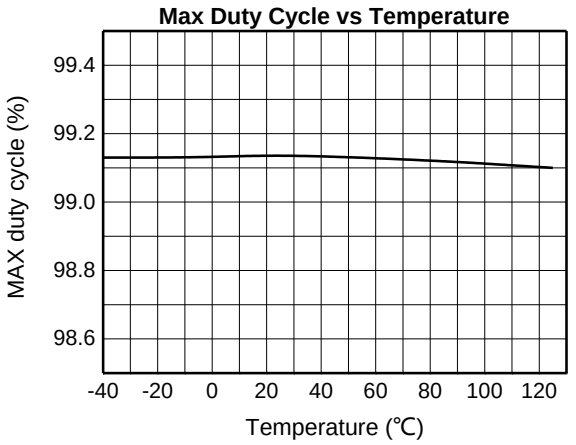
(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

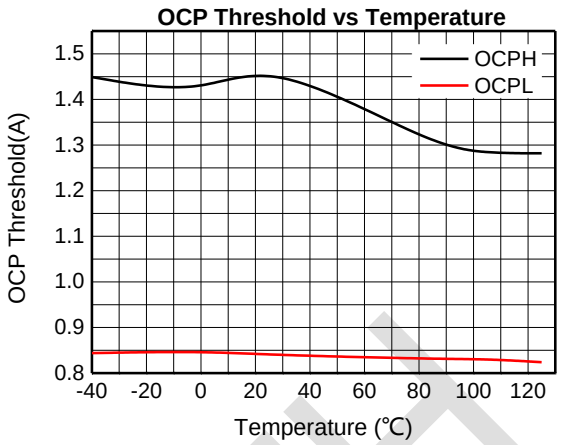
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3.8		24	V
Input undervoltage threshold	V_{UVLO}	VIN UP	3.4	3.6	3.8	V
Input undervoltage hysteresis	V_{UVLO_HYS}			300		mV
Input overvoltage threshold	V_{IN_OVP}	VIN Rise, Hysteresis = 1V	26	28	30	V
Input overvoltage protection hysteresis	$V_{IN\_OVP\_HYS}$			1		V
Input quiescent current	I_Q	IOUT=0, V_{FB} = V_{REF} x 105%		15		μA
Shutdown Current	I_{SHDN}	V_{IN} = 12V, EN = 0V		2		μA
FB Reference Voltage	V_{REF}		784	800	816	mV
FB Input Current	I_{FB}	V_{FB} = 2V		20		nA
Switching frequency	F_{OSC}		520	600	680	kHz
Minimum on-time	T_{ON_MIN}			80		ns
Maximum Duty Cycle	D_{MAX}			99		%
Foldback Frequency	F_{FB}	V_{FB} = 0.9 × V_{REF}		55		kHz
Upper Tube On Resistance	R_{LS_ON}	I_{SW} = 100mA		425		mΩ
Upper Current Limit	I_{LIMIT_HS}			1.5		A
Lower Tube On Resistance	R_{ON_LS}	I_{SW} = 100mA		270		mΩ
Lower tube current limit	I_{LIMIT_LS}			0.8		A
SW leakage current	I_{SW_lk}	V_{IN} = 12V, EN = GND			10	μA
EN Rising Threshold	V_{EN_H}	EN up		1.21		V
EN falling threshold	V_{EN_L}	EN down		1.17		V
EN input current	I_{EN}	V_{IN} = 12V, EN = 5V		1		μA
Soft start time	T_{SS}			1		ms
Output overvoltage protection		UP, V_{FB}/V_{REF}		110		%
		DOWN, V_{FB}/V_{REF}		105		%
Thermal shutdown threshold	T_{SHDN}	T_A rising		155		°C
Thermal shutdown hysteresis	T_{SHDN_HYS}			30		°C

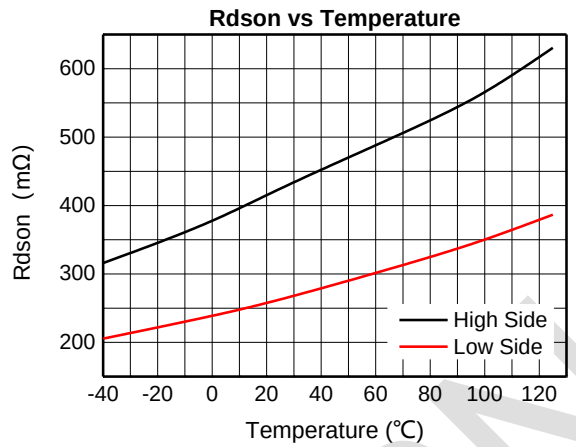
10.6 Characteristics Curve

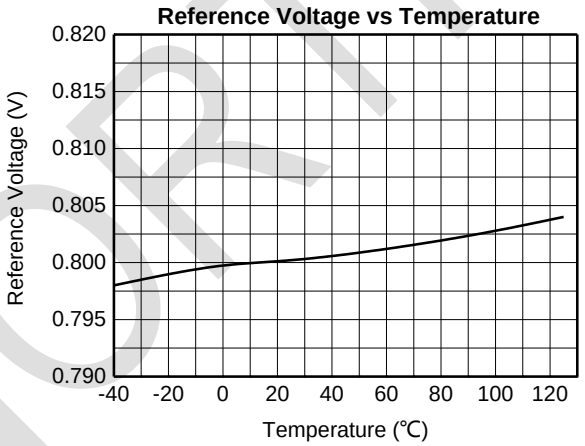
(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

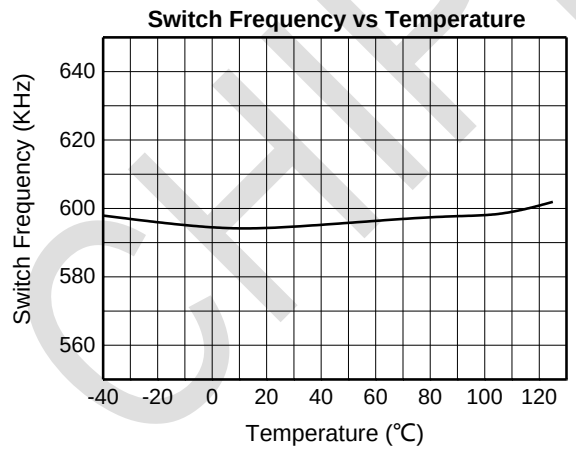


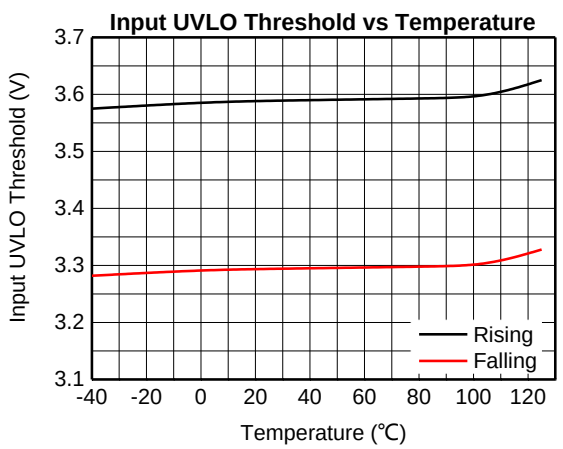

Max Duty Cycle vs Temperature
MAX duty cycle (%)
99.4
99.2
99.0
98.8
98.6
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


OCP Threshold vs Temperature
OCP Threshold(A)
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
OCPH
OCPL
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


Rdson vs Temperature
Rdson (mΩ)
600
500
400
300
200
High Side
Low Side
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


Reference Voltage vs Temperature
Reference Voltage (V)
0.820
0.815
0.810
0.805
0.800
0.795
0.790
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


Switch Frequency vs Temperature
Switch Frequency (KHz)
640
620
600
580
560
-40 -20 0 20 40 60 80 100 120
Temperature (℃)


Input UVLO Threshold vs Temperature
Input UVLO Threshold (V)
3.7
3.6
3.5
3.4
3.3
3.2
3.1
Rising
Falling
-40 -20 0 20 40 60 80 100 120
Temperature (℃)

11 Detailed Description

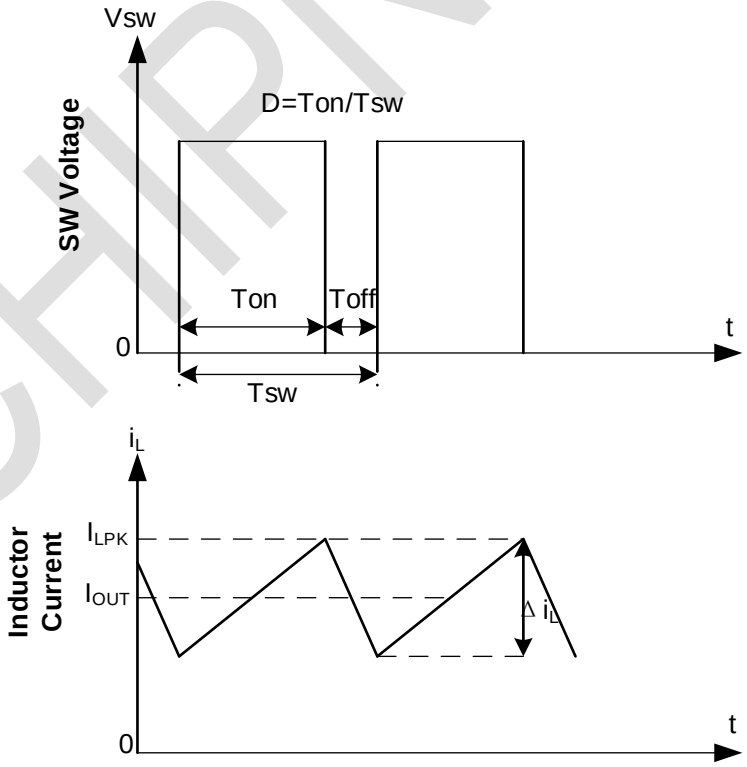
11.1 Overview

The CN2203TER is an easy-to-use synchronous buck converter with an input voltage range of 3.8V-24V and internal compensation to save external component count. At light load, the chip will enter PFM mode to maintain high efficiency operation; at heavy load, it will enter PWM mode to realize low ripple, excellent dynamic performance with fixed switching frequency. Enable and soft-start functions can meet the diversity of application scenarios. Few pins arrangement can simplify PCB layout.

11.2 Fixed Frequency Peak Current Control Mode

The CN2203TER is a synchronous buck converter that integrates an upper power MOS and a lower power MOS. It uses fixed-frequency current-mode control to control the on-time of the upper tube by detecting the peak current of the upper tube and comparing it to the output of the error amplifier in the voltage feedback loop. The voltage feedback loop has internal compensation, requires fewer peripheral devices, is simple to design, and various output capacitors can maintain stable operation. Under normal load conditions, the converter operates at a fixed switching frequency and under light load conditions, the converter will operate in PFM mode to maintain high efficiency.

The CN2203TER turns on and off the upper and lower MOS by controlling the duty cycle. During the on-time of the upper tube, the SW pin voltage rises to VIN and the inductor current IL increases at a linear slope (V_{IN}-V_{OUT})/L. When the upper tube is disconnected, the lower tube conducts after a dead time and the inductor current is renewed through the lower tube at a slope V_{OUT}/L. The control parameter of the buck converter is the duty cycle D = Ton/Tsw, where Ton is the upper tube conduction time and Tsw is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter with negligible peripheral device losses, D is proportional to the output voltage and inversely proportional to the input voltage: D = VOUT/VIN.



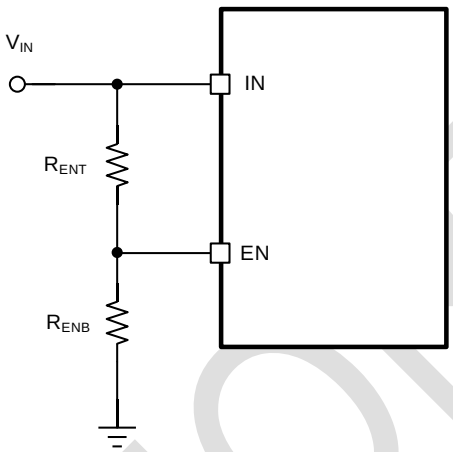
SW and inductor current waveforms in continuous conduction mode (CCM)

11.3 Enabling Startup

EN voltage control CN2203TER on and off, when EN voltage is higher than 1.21V, the chip starts; EN voltage is lower than 1.17V, the chip turns off. EN is an input pin, do not dangle or open circuit, the application can be connected to VIN to realize the chip self-start when the power supply system starts.

The system timing control can be realized by driving EN with an external logic signal, or by setting the UVLO of the power system by enabling the voltage divider resistors RENT and RENB, and the UVLO calculation formula is as follows:

$$V_{UVLO} = 1.21 * \left(\frac{R_{ENT}}{R_{ENB}} + 1\right)$$



Power System UVLO Setting

11.4 Minimum Off Time and Frequency Foldback

The minimum turn-off time (T_{OFF_MIN}) is the minimum time that the upper tube can be turned off. The typical value of T_{OFF_MIN} for the CN2203TER is 200ns, and T_{OFF_MIN} will limit the voltage conversion range when in CCM mode and without frequency foldback.

The maximum duty cycle without frequency foldback is:

$$D_{MAX} = 1 - T_{OFF\_MIN} * f_{SW}$$

The minimum VIN without foldback frequency for a given output voltage can be calculated by the following equation:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{sw} * T_{OFF_{MIN}}}$$

The foldback frequency is suitable when a larger duty cycle is required under low VIN conditions. After triggering T_{OFF_MIN}, the frequency starts to decrease and the duty cycle can be increased according to the D_{MAX} formula. In this case, the frequency can be reduced to 55 KHz. the wide frequency foldback range enables the CN2203TER output voltage to be stabilized with a large reduction in VIN.

11.5 Bootstrap Voltage

The CN2203TER has an integrated bootstrap regulator with a bootstrap capacitor placed between the BST pin and the SW pin. The bootstrap regulator charges the bootstrap capacitor when the upper tube is disconnected and the lower tube is on, and the bootstrap capacitor provides the drive voltage for the upper tube when the lower tube is disconnected and the upper tube is on. A commonly used ceramic capacitor with a rated voltage of 50V 0.1uF (X5R or X7R) can be used to ensure stable performance over the entire temperature and voltage range.

11.6 Overcurrent and short-circuit protection

The CN2203TER has cycle-by-cycle peak and valley inductor current limiting to provide overcurrent and short-circuit protection for the device and to limit the maximum output current. When the upper tube is energized, the upper tube current is detected. During each switching cycle, the upper tube current is compared with the output of the error amplifier minus the slope compensation, and when the upper tube current reaches the peak current limit threshold of 1.5A, the upper tube is disconnected and the lower tube is energized to reduce the inductor current. When the lower tube is energized, the lower tube current is detected. If the lower tube current is higher than the valley current limit threshold of 0.8A, the lower tube will not be disconnected at the end of the switching cycle, and it will remain energized until the inductor current decreases to 0.8A, and then the lower tube is disconnected and the upper tube is energized.

If the overcurrent continues for 1ms, or VFB<65%*Vref, it will enter hiccup mode, the chip will disconnect the upper and lower MOS when it enters hiccup mode, and then it will start softly after 8ms, if the overcurrent or short-circuit state still exists, the hiccup mode will be repeated until the overcurrent or short-circuit disappears.

11.7 FB short circuit protection

The FB short-circuit protection prevents damage to the power system's back-end circuits from excessive output voltage during an FB short-circuit. When any protection is activated or triggered, the chip will detect the resistance between the FB pin and GND, if this resistance is less than 400Ω, the upper and lower MOS will stop switching until the short circuit disappears.

11.8 Soft Start

The soft-start function suppresses input surges during power supply startup, minimizing the impact on the chip and the input power supply. Soft-start is achieved by slowly ramping up the internal reference voltage during chip power-up, with a typical time of 1ms.

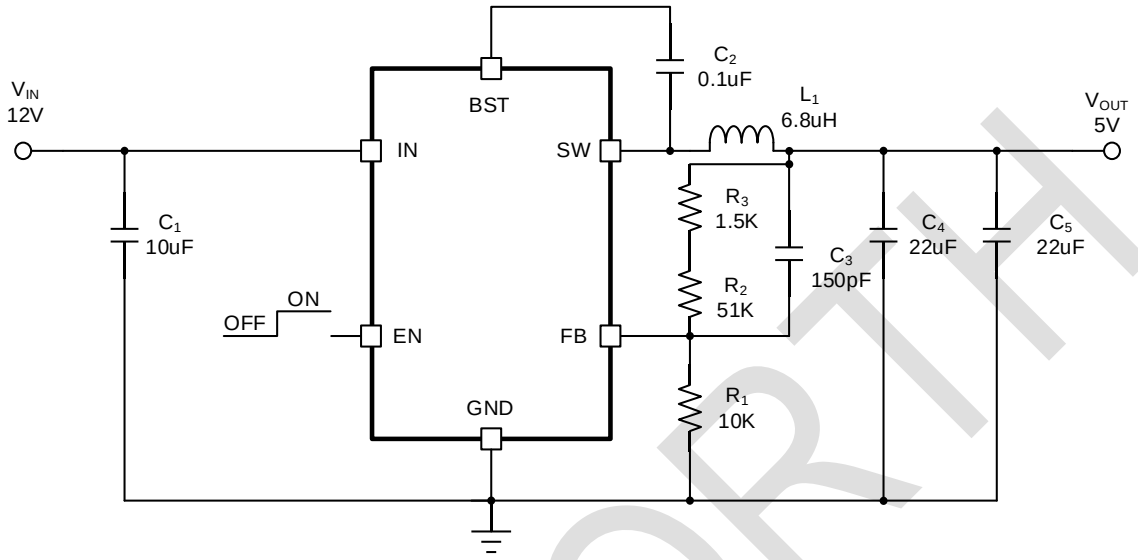
11.9 Thermal shutdown

The CN2203TER has an internal thermal shutdown function. When the internal junction temperature of the chip exceeds 155°C, the upper and lower MOS will stop switching to reduce the junction temperature, and the chip will restart softly when the junction temperature is reduced to 125°C or less.

12 Application information

12.1 Typical applications

The following figure shows a typical application schematic for a circuit that can be used as a means of evaluating the performance of the CN2203TER.



Application Schematic

12.2 Design requirements

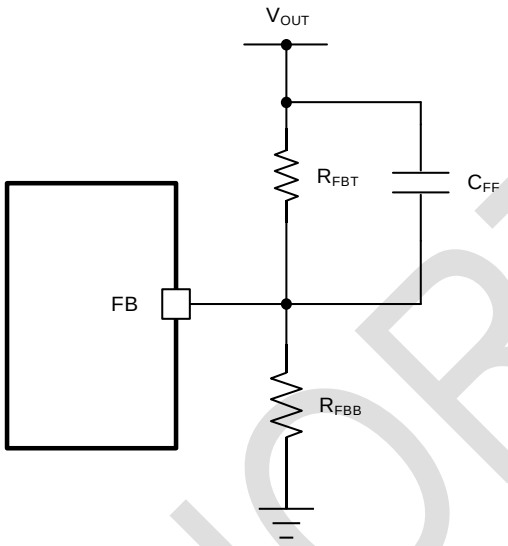
Indicator	Minimum	Typical	Maximum	Unit
5V Output	4.75	5	5.25	V
Input Voltage	6.5	12	24	V
Output Ripple			10	mV

12.3 Design process

12.3.1 Output voltage

The internal reference voltage of CN2203TER is 0.8V, the output voltage can be set by voltage divider resistor, it is recommended to use the resistor with 1% error and low temperature coefficient. The output voltage formula can be used to select the appropriate pull-up resistor R_{FBT} and pull-down resistor R_{FBB}, it is recommended that the resistance value of R_{FBB} is in the range of 10K-50K. the formula is as follows:

$$V_{OUT} = 0.8 * \left(\frac{R_{FBT}}{R_{FBB}} + 1\right)$$



Output Voltage Setting

The feedforward capacitor C_{FF} is connected in parallel with the R_{FBT} to produce a zero and a pole, distributed before and after the loop crossing frequency, which is used to improve the phase margin of the loop, and it is recommended that this zero is 20 KHz, and the zero is calculated by the following formula:

$$f_{Z\_CFF} = \frac{1}{2\pi * R_{FBT} * C_{FF}}$$

In a typical application, R_{FBB} selects 10K, R_{FBT} selects 51K in series with 1.5K, and C_{FF} selects 150pF.

12.3.2 Inductors

The formula for calculating inductor selection is as follows:

$$L = \frac{V_{OUT}}{f_S * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- fs is the switching frequency
- ΔIL is the inductor ripple current, typically 30% of the load current
- I_{OUT} is the load current

The main parameter for inductor selection is the saturation current of the inductor, which must be higher than the peak inductor current calculated by the design with an additional 20% margin. The peak inductor current is calculated using the following formula:

$$IL_{PEAK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{2 * V_{IN} * L * f_s}$$

Another important parameter is the inductor temperature rise current, which needs to be higher than the output current with an additional 20% margin, on which a lower DC resistance inductor is used as much as possible to improve efficiency.

12.3.3 Output Capacitor Selection

Output capacitor selection is very important, because it directly affects the output ripple, loop stability, transient response of the upstroke and downstroke. Selection needs to pay attention to the piezoelectric effect of capacitors, try to use ceramic capacitors, in typical applications it is recommended to use two 22uF ceramic capacitors in parallel.

As the ceramic capacitor parasitic ESR and ESL is very small, can be ignored, the output ripple ΔV_O is mainly determined by the capacitance capacity, the formula is:

$$\Delta V_O = \frac{\Delta I_L}{8 * f_s * C_{OUT}}$$

Transient response, when the light load quickly becomes heavy load, the output capacitance needs to supply current to the load before the loop adjusts the inductor current to the appropriate current. Loop control generally requires at least 5 cycles to adjust the inductor current to the current state corresponding to the heavy load, so the output capacitance has to be large enough to supply power to the load within 5 cycles and ensure that the downstroke voltage is within the specification. The following formula can be used to calculate the minimum output capacitance required to meet the downstroke specification:

$$C_{OUT} > \frac{5 * (I_{OH} - I_{OL})}{f_s * V_{US}}$$

When a heavy load quickly changes to a light load, the output capacitance needs to absorb the energy stored in the inductor, resulting in an output voltage upstroke. The following formula calculates the minimum output capacitance required to meet the upstroke specification:

$$C_{OUT} > \frac{{I_{OH}}^2 - {I_{OL}}^2}{(V_{OUT} + V_{OS})^2 - {V_{OUT}}^2} * L$$

- I_{OH} is heavy load during transient response
- I_{OL} is light load for transient response
- V_{US} is the downstroke specification for transient response
- V_{OS} is the upstroke specification of transient response

12.3.4 Bootstrap Capacitor Selection

The CN2203TER requires a bootstrap capacitor to provide drive voltage to the upper tube. It is recommended to connect a 0.1uF low ESR ceramic capacitor between BST-SW.

12.3.5 Bill of materials

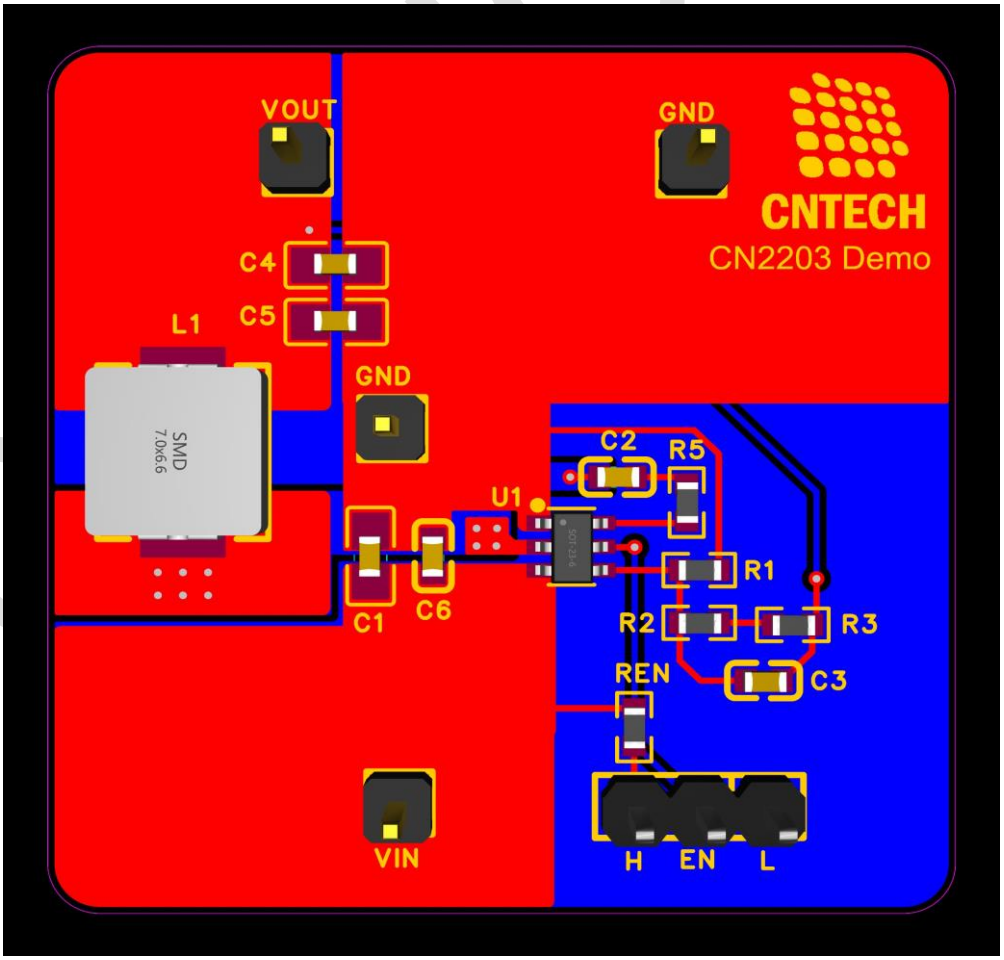
Symbol	Description	Manufactures	Part Number	Qty
C1	10uF ±10%, 50V, X5R	YAGEO	CC1206KKX5R9BB106	1
C2	100nF ±10%, 50V, X7R	YAGEO	CC0603KRX7R9BB104	1
C3	150pF ±10%, 50V, X7R	YAGEO	CC0603KRX7R9BB151	1
C4,C5	22uF ±20%, 25V, X5R	YAGEO	CC0805MKX5R8BB226	2
L1	6.8uH ±20%, Isat:3.4A	TDK	SPM5030T-6R8M-HZ	1
R1	10kΩ ±1%, 100mW, ±100ppm/°C	UNI-ROYAL	0603WAF1002T5E	1
R2	51kΩ ±1%, 100mW, ±100ppm/°C	UNI-ROYAL	0603WAF5102T5E	1
R3	1.5kΩ ±1%, 100mW, ±100ppm/°C	UNI-ROYAL	0603WAF1501T5E	1

12.4 PCB Layout Guidelines

Layout is an important step for all switching power supplies, especially in the case of high peak currents with high frequencies, and a layout that is not carefully done may have an effect on the stability of the converter as well as on electromagnetic interference. Here are some suggestions for layout and wiring:

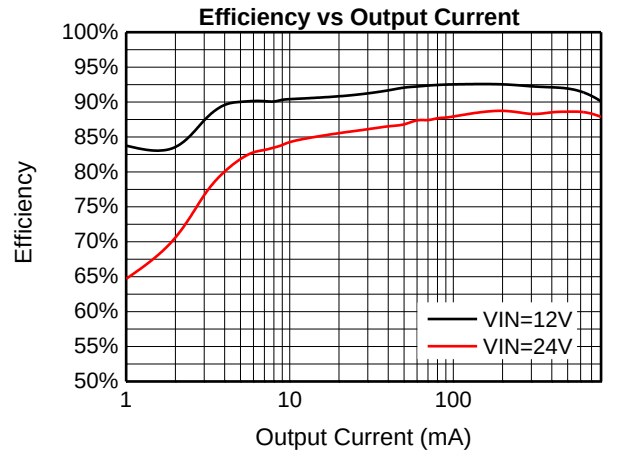
- Upper tube conduction loop, lower tube conduction loop should be as small as possible, especially the upper tube and lower tube parasitic diode common-pass loop to be small, the specific approach is the input capacitance, especially small capacitance (eg, 100nF) to be close to the chip's VIN and GND, output capacitance should be close to the inductance and the chip GND
- Inductors should be placed close to the SW
- VOUT feedback line away from the inductor and SW and other sources of interference, and in the alignment on both sides of the ground shielding filtering
- Signal and power parts should be separated to avoid interference by the power loop electromagnetic coupling, refer to the datasheet is separated from the top and bottom, the signal part of the following, the power part of the above
- The bottom ground plane as far as possible to complete, less cutting
- Input and output positive and negative terminals, should be placed close to the input and output capacitors, especially the GND terminal, can not be placed arbitrarily, will affect the actual path of the current return, affecting layout effect

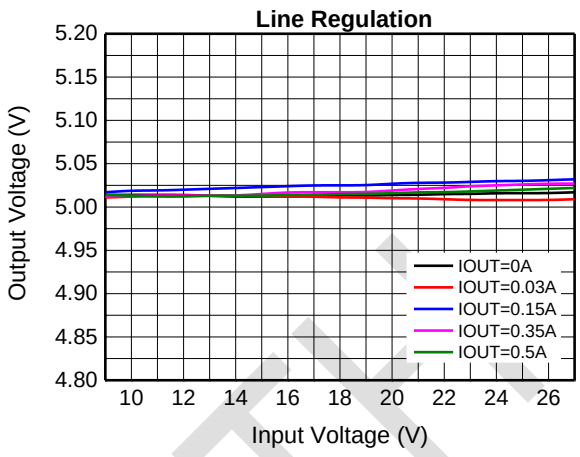
In addition, the need to add power or signal points to be measured, it is best to lead out and connect to the terminals to facilitate the test, pay attention to these connections also do not arbitrarily line, but also refer to the above principles to avoid interference and be interfered with.

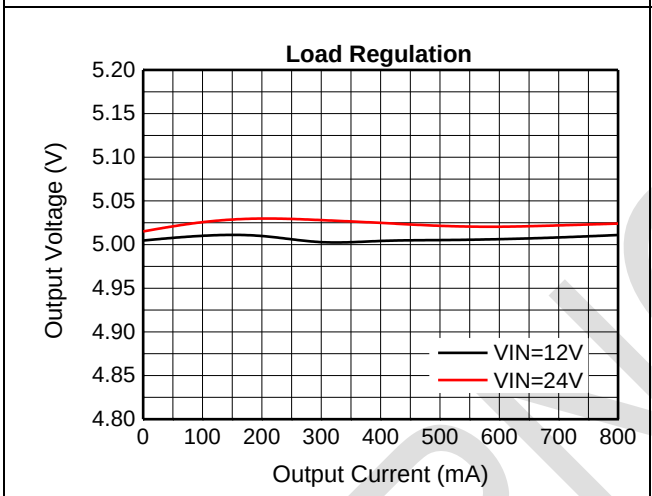


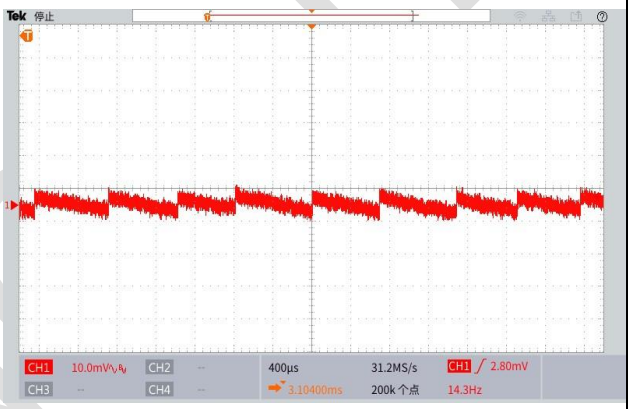
12.5 Basic Performance

(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

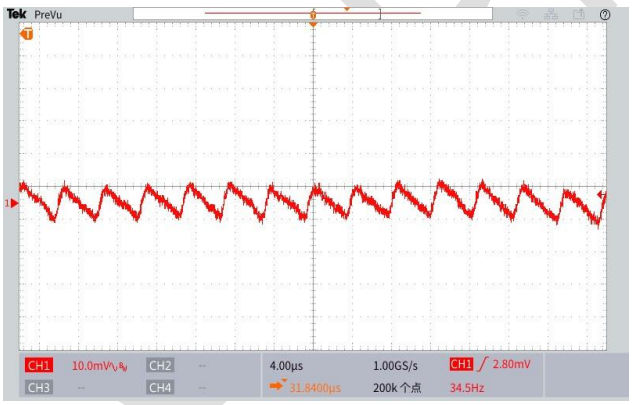




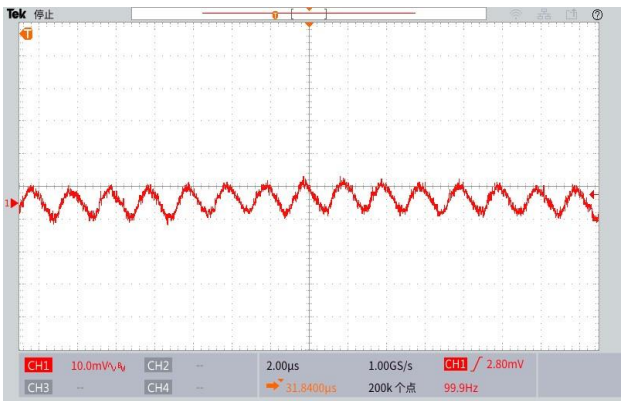




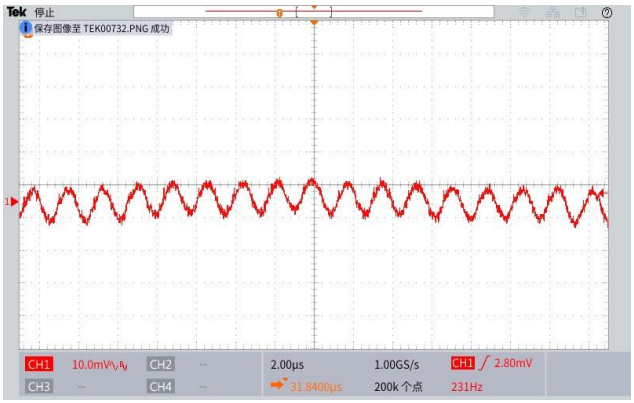
IOUT=0A,Output ripple



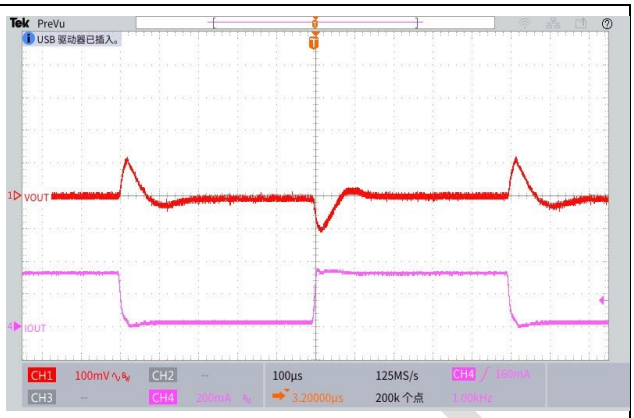
IOUT=0.05A,Output ripple



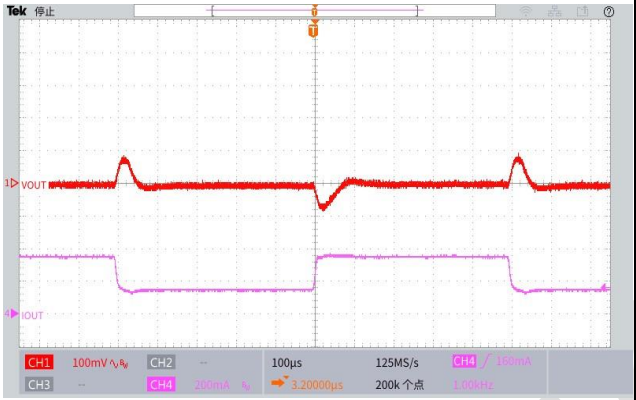
IOUT=0.15A,Output ripple



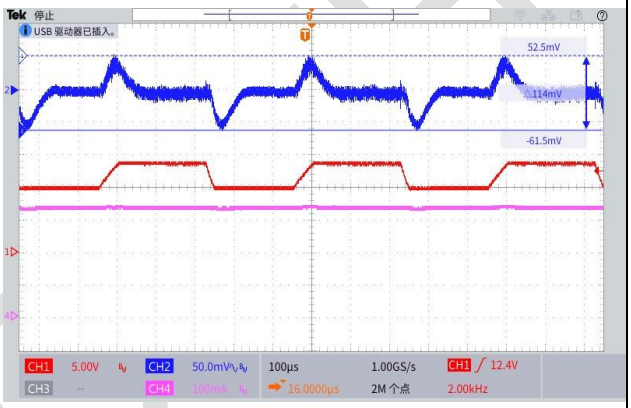
IOUT=0.35A,Output ripple



IOUT=0.05A-0.35A



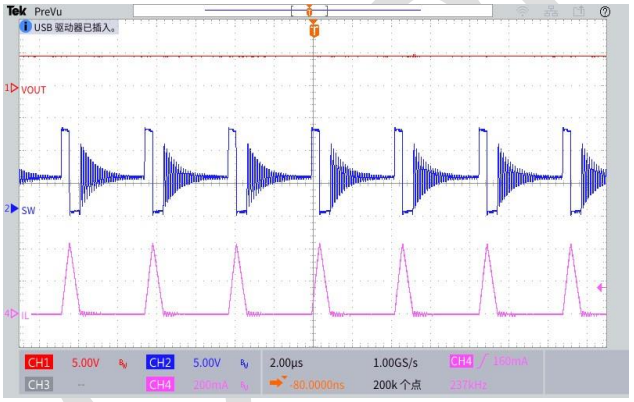
IOUT=0.15A-0.35A



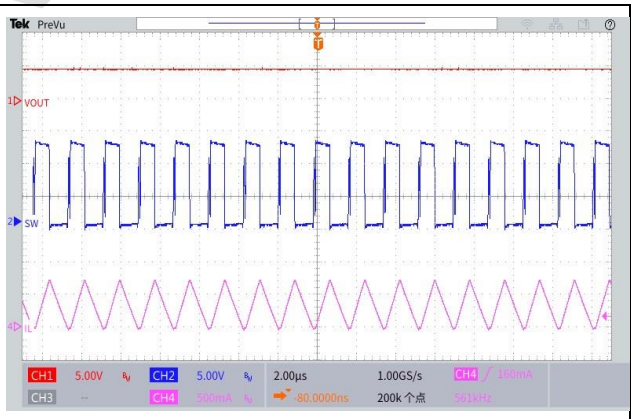
VIN=10V-14V,IOUT=0.35A

12.6 Operating waveforms

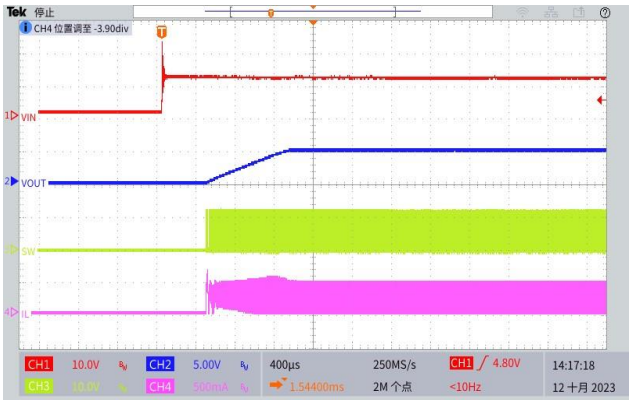
(V_{IN}=12V, T_A=25°C, unless otherwise specified.)



IOUT=0.05A,PFM Mode



IOUT=0.35A,PWM Mode



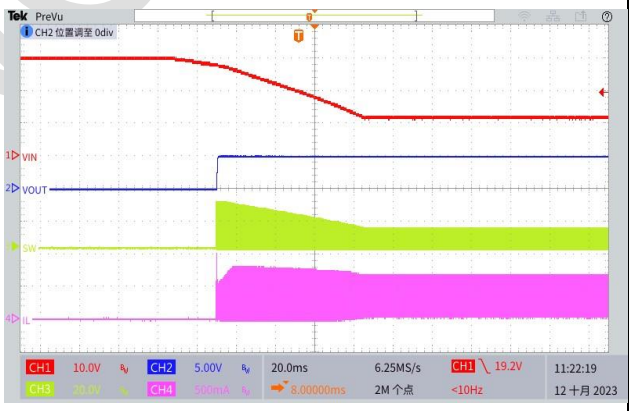
IOUT=0.15A,VIN UP

IOUT=0.35A,VIN UP

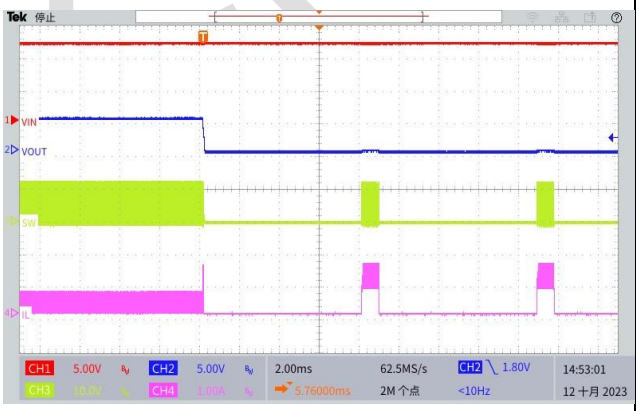
IOUT=0.15A,VIN DOWN

IOUT=0.35A,VIN DOWN

VIN OVP Protection



VIN OVP Recover

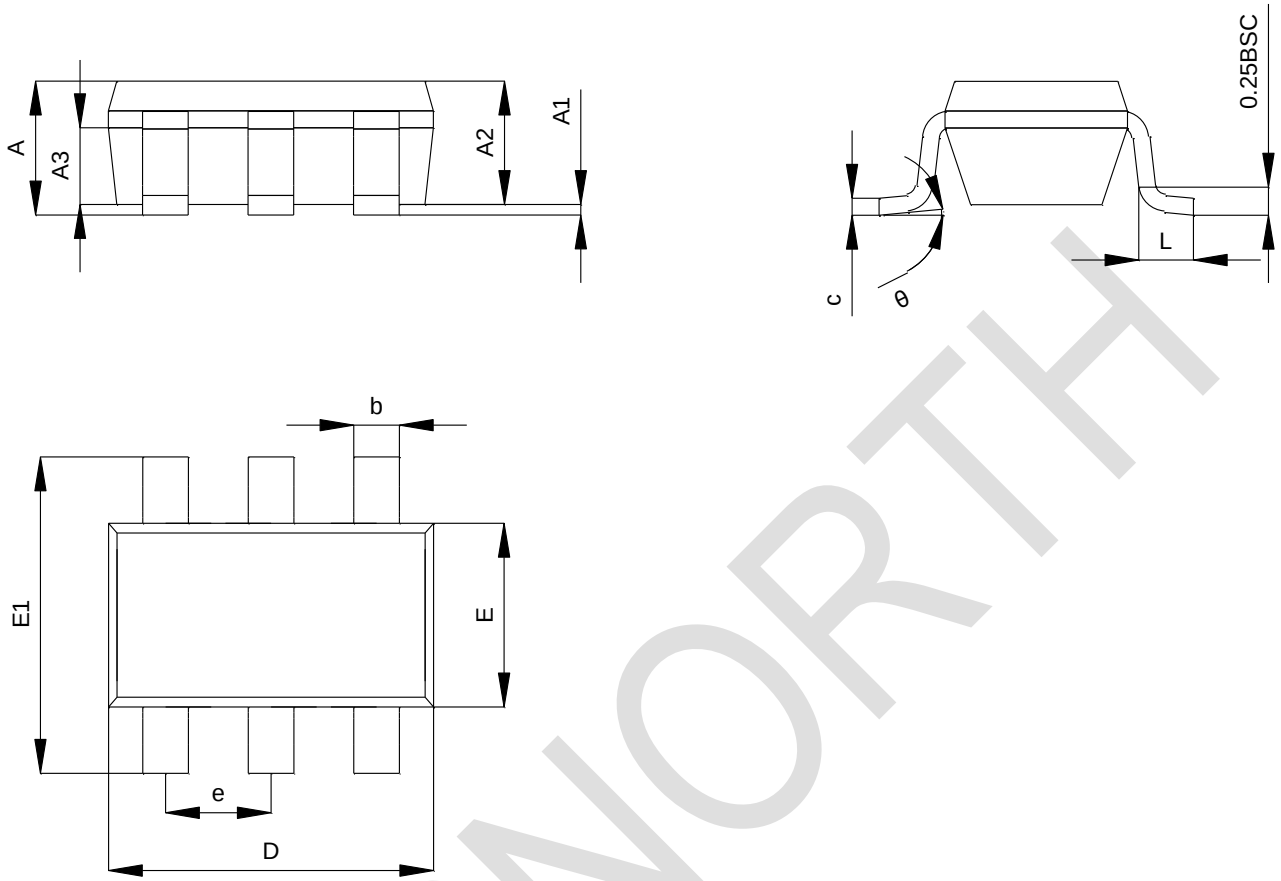


OCP Protection

OCP Recover

13 Package Information

SOT23-6L



SYMBOL	Millimeter		
	MIN	MON	MAX
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E	1.510	1.610	1.700
E1	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

14 Important Statement

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