800KHz, 18V Input, 2A Output Current Synchronous Buck Converter

1 Description

The CN2202TER is a high efficiency DC-DC synchronous buck converter, capable of delivering up to 2A output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from heavy load to light load. During light load, CN2202TER goes into a PFM mode that saves switching loss achieving high efficiency. The adaptive COT control also maintains a constant switching frequency across line and load.

CN2202TER is available in SOT23-6L package.

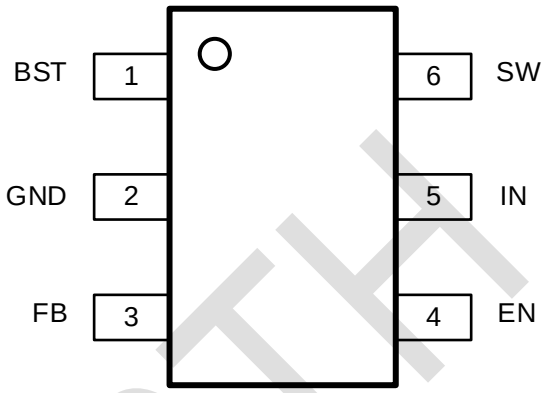
2 Features

- 4.5V to 18V Wide Input Operating Range
- 19V Input Over Voltage Protection
- Capable of Delivering 2A
- Efficiency up to 92%
- No load Iq 100uA
- 600mV ±2% Feedback reference voltage
- 800kHz fixed frequency
- Adaptive COT Control
- High Efficiency PFM mode at light load
- Hiccup mode over current protection and short circuit protection
- Cycle-by-cycle peak and valley current limiting
- 1ms internal soft start
- Thermal Shutdown and UVLO

3 Applications

- LCD TV
- Set-top boxes
- xDSL modems

4 Pin Definition



SOT23-6L

5 Ordering Information

Product Number	Package	Quantity/Tape
CN2202TER	SOT23-6L	3000pcs

6 Marking

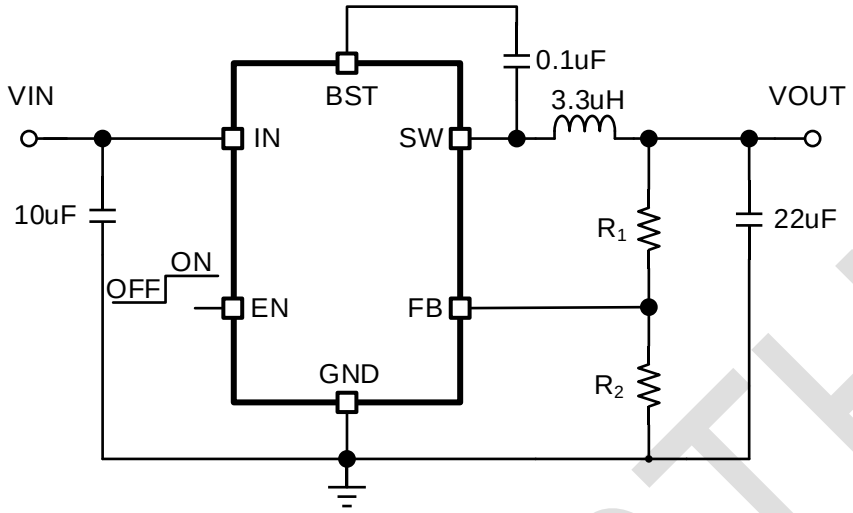
Product Number	Marking
CN2202TER	CN2202 YYWW

Green (RoHS & HF)：CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL)：3

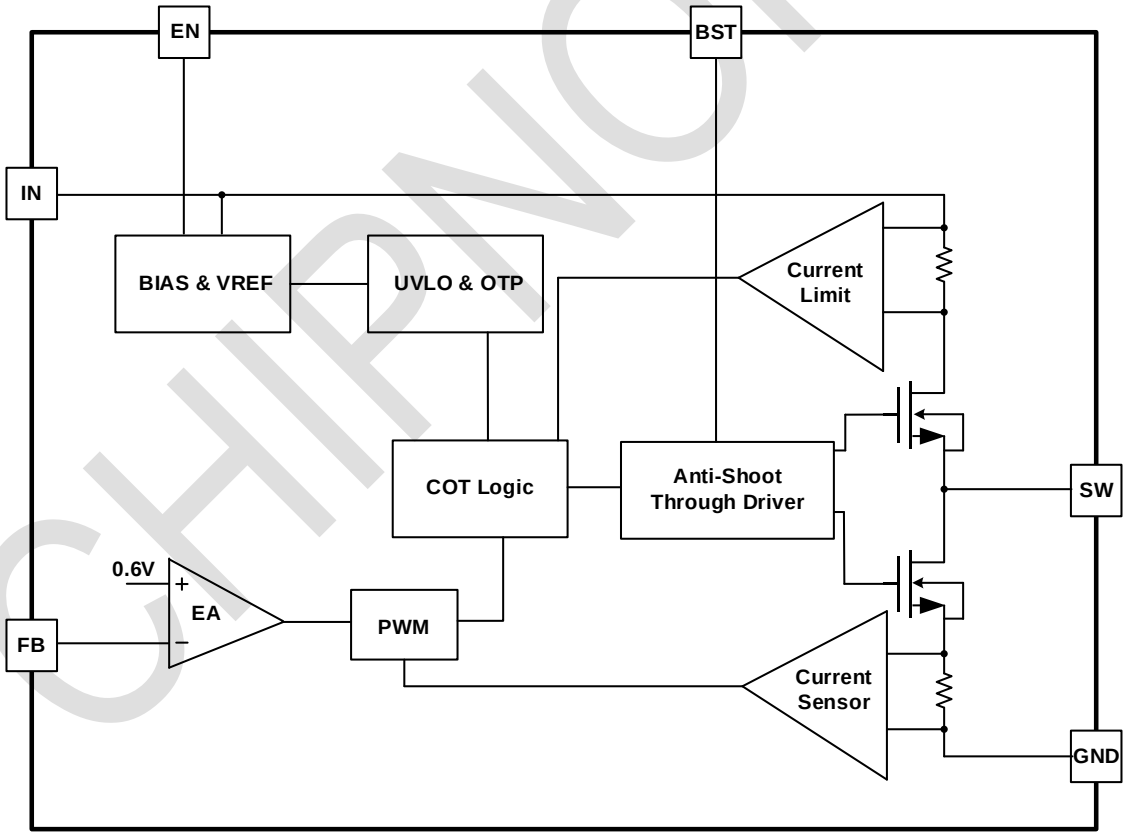
Note：YY=Year WW=Week.

7 Typical Application



Note 1: $V_{OUT} = V_{REF} \times (R_1+R_2) / R_2$

8 Block Diagram



9 Pin Descriptions

Pin No.	Pin Name	Descriptions
1	BST	Bootstrap pin. Connect a 100nF capacitor between BST and SW
2	GND	Ground.
3	FB	Feedback pin. Connect FB to the center point of external resistor divider from VOUT to GND
4	EN	Enable pin, active high. Drive this pin high to enable the part, low or floating to disable.
5	VIN	Power supply input. Bypass with a 10μF capacitor from V_{IN} to GND as close as possible to IC pin.
6	SW	Switch node pin. Connect an inductor between SW and COUT/VOUT.

10 Specifications

10.1 Absolute Maximum Ratings(2)

Parameter	Symbol	Value	Units
Supply Input Voltage	V_{IN}	-0.3 ~ 30	V
SW, EN Voltage	VSW, VEN	-0.3 ~ V_{IN} + 0.3	V
Bootstrap BST Voltage	VBST	-0.3 ~ V_{SW} + 6	V
FB Voltage	VFB	-0.3 ~ 6	V
Operating Junction Temperature Range	T_J	-40 ~ 150	°C
Operating Ambient Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{STG}	-55 ~ 150	°C
Lead Temperature(soldering 10s)	T_{LEAD}	260	°C

Note2: Stress exceeds these ratings listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability.

10.2 ESD Ratings

Discharge mode	Value	Units
HBM	±4000	V
CDM	±2000	V

10.3 Recommended Operating Range

Parameter	Symbol	Min.	Max.	Units
Operating Voltage Range	V_{IN}	4.5	18	V
Input Capacitor Range	C_{IN}	10		μF
Output Capacitor Range	C_{OUT}	22		μF
Bootstrap Capacitor Range	C_B	100		nF
Inductor Range	L	2.2	4.7	μH

10.4 Thermal Information

Parameter	Descriptions	Value	Unit
$R_{\theta JA}$	Junction to ambient	173	°C/W
$R_{\theta JC}$	Junction to case	116	°C/W

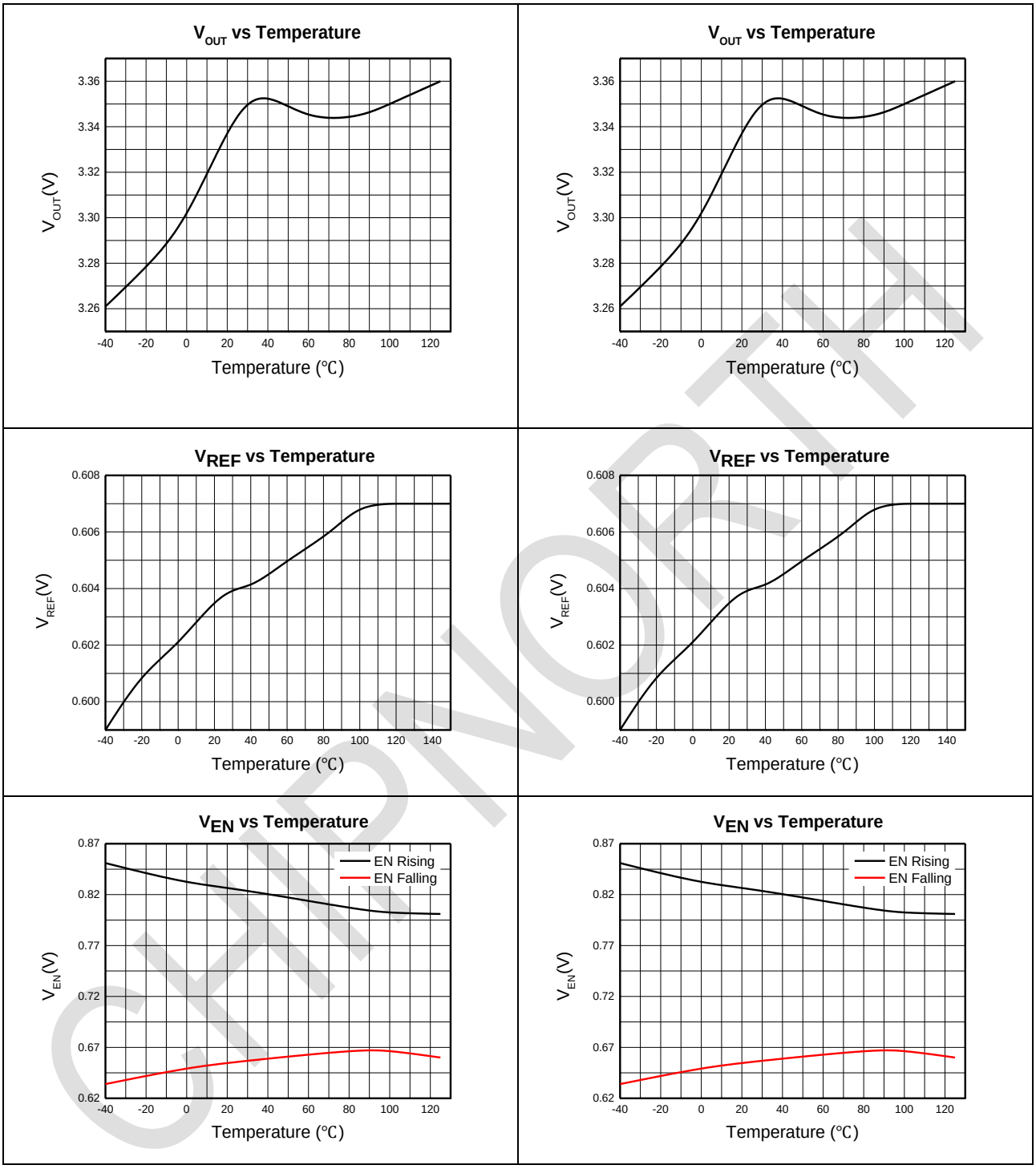
10.5 Electrical Characteristics

(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage Range	V_{IN}		4.5		18	V
Input UVLO Threshold	V_{UVLO_R}	V_{IN} Rising, Hysteresis = 300mV	4	4.2	4.4	V
Input OVP Threshold	V_{IN_OVP}	V_{IN} Rising, Hysteresis = 1V	18.2	19	19.8	V
Input Quiescent Current	I_Q	No load, V_{FB} = V_{REF} x 105%		80	122	μA
Shutdown Current	I_{SHDN}	V_{IN} = 12V, EN = 0V		1.8	4.8	μA
FB Reference Voltage	V_{REF}		588	600	612	mV
FB Input Current	I_{FB}	V_{FB} = 2V		0	0.5	uA
Switching Frequency	F_{OSC}		610	800	990	kHz
Minimum On Time	T_{ON_MIN}			100		ns
Minimum Off Time	T_{OFF_MIN}			125		ns
Maximum Duty Cycle	D_{MAX}			90		%
High Side On-Resistance	R_{ON_HS}	I_{SW} = 100mA		170		mΩ
Low Side On-Resistance	R_{ON_LS}	I_{SW} = 100mA		105		mΩ
Low Side Current Limit	I_{LIMIT_LS}		2	3	4	A
SW Leakage Current	I_{SW_lk}	V_{IN} = 12V, EN = GND			0.5	μA
EN Rising Threshold	V_{EN_R}	Rising	1.2			V
EN Falling Threshold	V_{EN_F}	Falling			0.4	V
EN Input Current	I_{EN}	V_{IN} = 12V, EN = 2V		2.5		μA
Soft-Start Time	T_{SS}			1		ms
Thermal Shutdown Temperature	T_{SHDN}	Rising, Hysteresis = 30°C		160		°C

10.6 Characteristics Curve

(V_{IN}=12V, V_{OUT}=3.3V, TA= 25°C, unless otherwise noted.)



11 Detailed Description

11.1 Overview

CN2202TER is a wide input range, high efficiency and high frequency DC to DC step down switching regulator, capable of delivering up to 2 A of output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. It compares the sum of the FB voltage and a ripple voltage that mimics the voltage due to the output ESR and capacitance. The constant on time timer varies with line to achieve relative constant switching frequency across line.

11.2 Control Mechanism

The CN2202TER utilizes current-mode control to regulate the FB voltage. Voltage at the FB pin is regulated at 0.6V so that by connecting an appropriate resistive divider between VOUT and GND, designed output voltage can be achieved.

11.3 Light Load Operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFET, power is lost due to the finite R_{dson} of the MOSFET and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. CN2202TER goes into a power save mode during light load, thereby extending the range of high efficiency operation.

11.4 Functional Descriptions

11.4.1 Enable

EN is a digital control pin that turns the CN2202TER on and off. Drive EN High to turn on the regulator, drive it Low to turn it off. An internal 1MΩ resistor from EN pin to GND allows EN to float to shut down the chip. Connecting the EN pin through a pull up resistor or shorted EN to IN will automatically turn on the chip whenever plug in IN.

11.4.2 Over Current Protection and Hiccup

CN2202TER has a cycle-by-cycle over current limit for when the inductor current peak value is over the set current limit threshold. When the output voltage drop until FB falls below UV threshold (0.3V), the CN2202TER will enter hiccup mode. It will turn off the chip immediately for 6mS. After that, it will try to re-starts as normal for 1mS. After 1mS, if FB is still below UV threshold, then the chip enters hiccup mode again. If FB is higher than UV threshold, it will enter the normal mode.

11.4.3 Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool down. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

11.4.4 Internal Soft-Start.

Soft-Start makes output voltage rising smoothly follow an internal SS voltage until SS voltage is higher than the internal reference voltage. It can prevent overshoot of output voltage when startup.

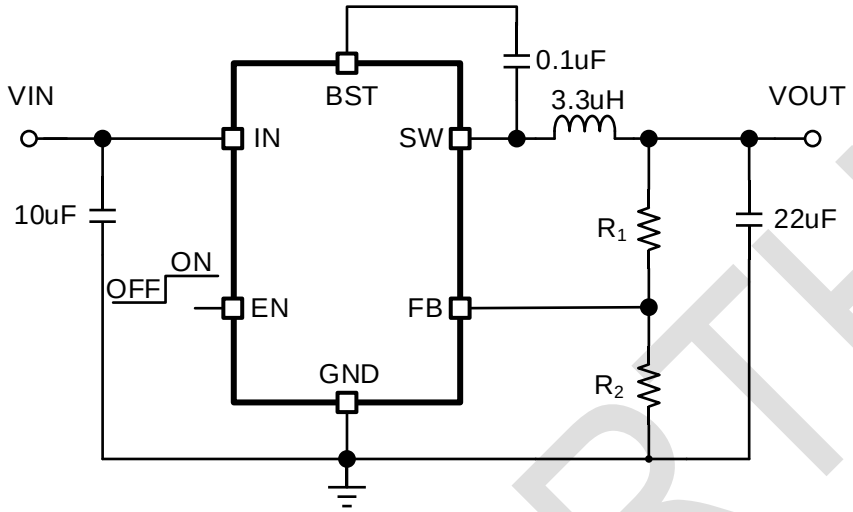
11.4.5 V_{IN} Under-Voltage Protection

A resistive divider can be connected between V_{IN} and GND, with the central tap connected to EN, so that when V_{IN} drops to the pre-set value, EN drops below 1.8V to trigger input under voltage lockout protection.

12 APPLICATION INFORMATION

12.1 Typical Application

The following figure shows a typical application schematic for a circuit that can be used to evaluate the performance of the CN2202TER.



12.2 External Output Voltage Setting

In external Output Voltage Setting Version selected, the CN2202TER regulator is programmed using an external resistor divider. The output voltage is calculated using below equation.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where: VREF =0.6V typically (the internal reference voltage)

Resistors R2 has to be between 1kOhm to 70KOhm and thus R1 is calculated by following equation

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2$$

12.3 Selecting the Inductor

A DC current rating of at least 20% percent higher than the maximum load current is recommended for most applications. Inductance value is related to inductor ripple current value, input voltage, output voltage setting and switching frequency. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔI_L is inductor ripple current. Large value inductors result in lower ripple current and small value inductors result in high ripple current, so inductor value has effect on output voltage ripple value. DC resistance of inductor which has impact on efficiency of DC/DC converter should be taken into account when selecting the inductor. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions, larger inductance is recommended for improved light load efficiency.

12.4 Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_s \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

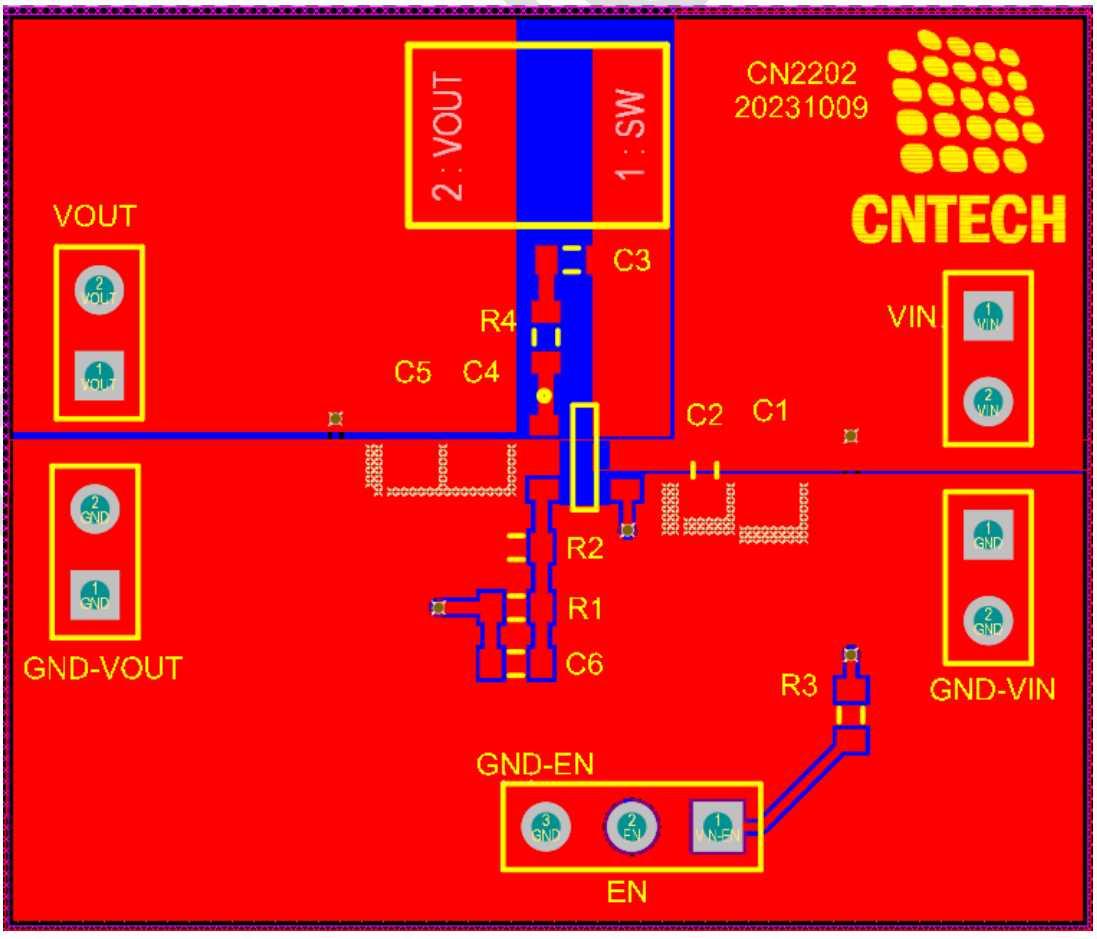
The characteristics of the output capacitor also affect the stability of the regulation system. The CN2202TER can be optimized for a wide range of capacitance and ESR values.

12.5 PCB Layout Guides

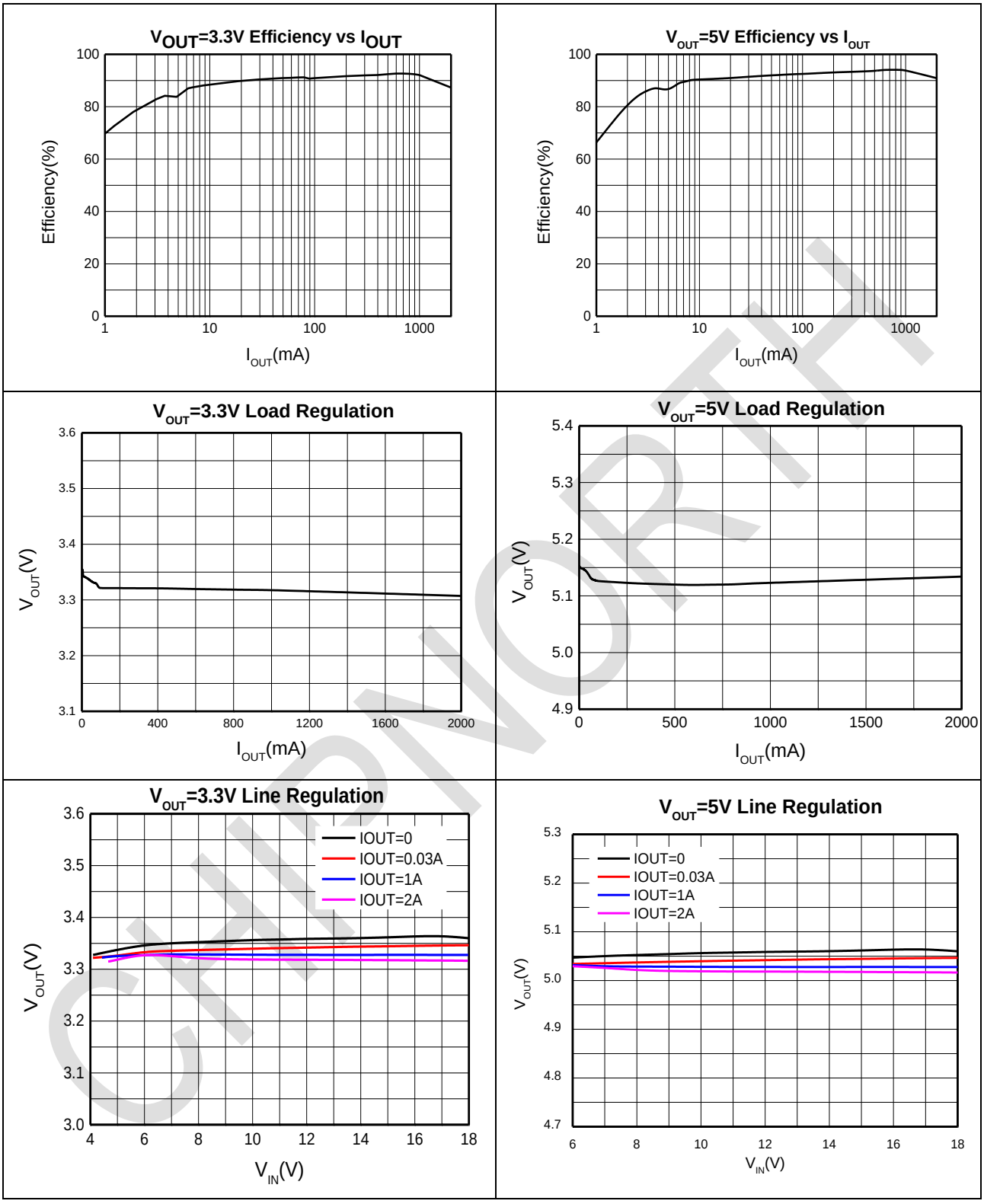
Layout is an important step for all switching power supplies, especially in the case of high peak currents with high frequencies, and a less careful layout may have an effect on the stability of the converter as well as electromagnetic interference. The following are some suggestions for layout and wiring:

- The upper tube conduction loop, the lower tube conduction loop should be as small as possible, especially the upper tube and the lower tube parasitic diode common loop should be small, the specific approach is the input capacitance, especially small capacitance (100nF) to be close to the chip's V_{IN} and GND, the output capacitance should be close to the inductance and the chip's GND.
- Inductor should be placed close to SW.
- Keep the VOUT feedback line away from interference sources such as inductor and SW, and place ground shielding and filtering on both sides of the line.
- The signal part and power part should be separated to avoid interference by electromagnetic coupling of the power circuit, refer to the datasheet which is separated from the top and bottom. The signal part is at the bottom and the power part is at the top.
- Ground floor plan to be finished as much as possible with less cutting.
- The positive and negative terminals of the input and output should be placed close to the input and output capacitors respectively, especially the GND terminal, which should not be placed arbitrarily and will affect the actual path of current return. This will affect the actual path of current return and affect the layout effect.

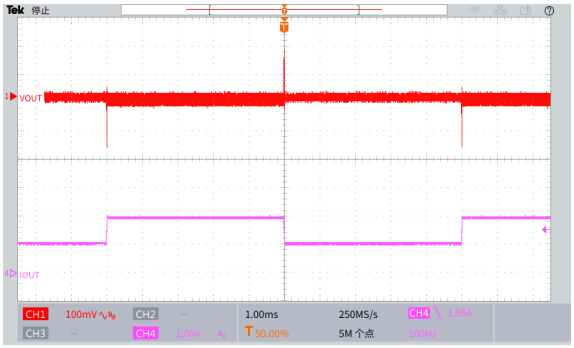
In addition, the need to add power or signal points to be measured, it is best to lead out and connect to the terminals to facilitate the test, pay attention to these wires are also Do not arbitrarily route, also refer to the above principles to avoid interference and be interfered with.



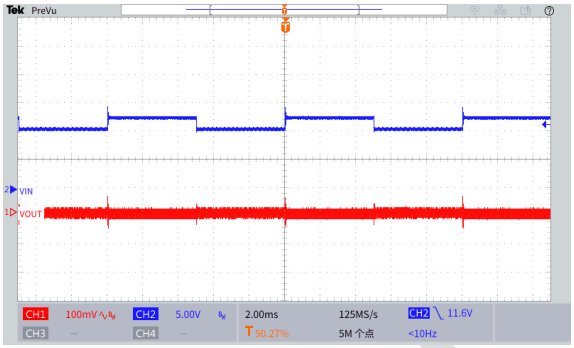
12.6 Basic Performance



Load Transient Response



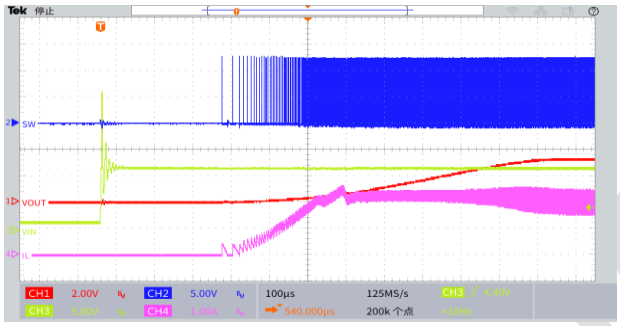
Line Transient Response



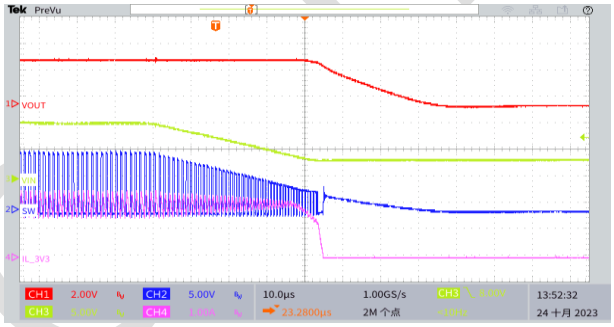
12.7 Working Waveforms

Test conditions: T_A=25°C, L=3.3μH, C_{IN}=C_{OUT}=10μF, unless otherwise specified.

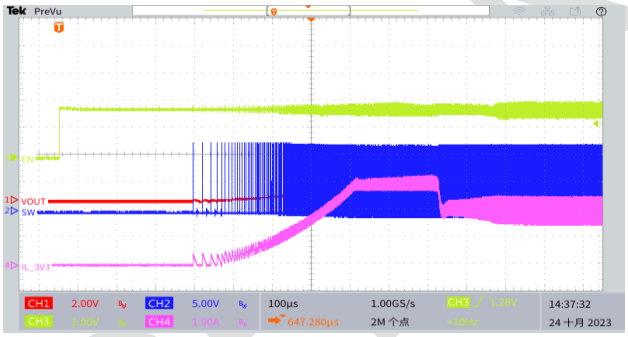
Start-Up From VIN



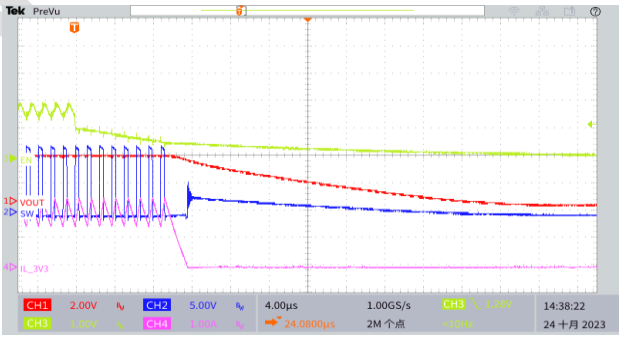
Shut-Down From VIN



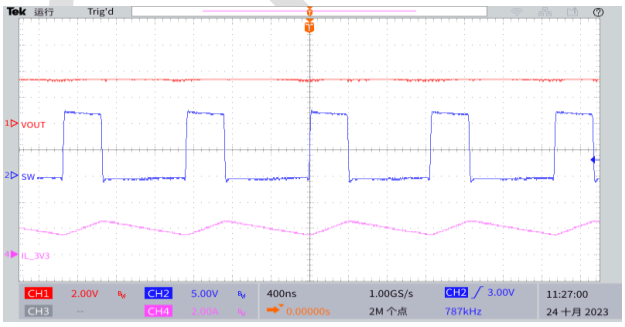
Start-Up From EN



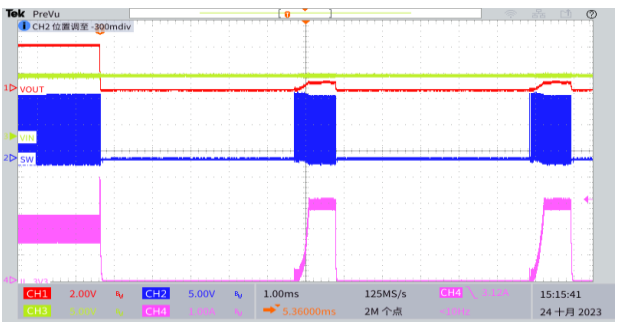
Shut-Down From EN



Operation Waveforms

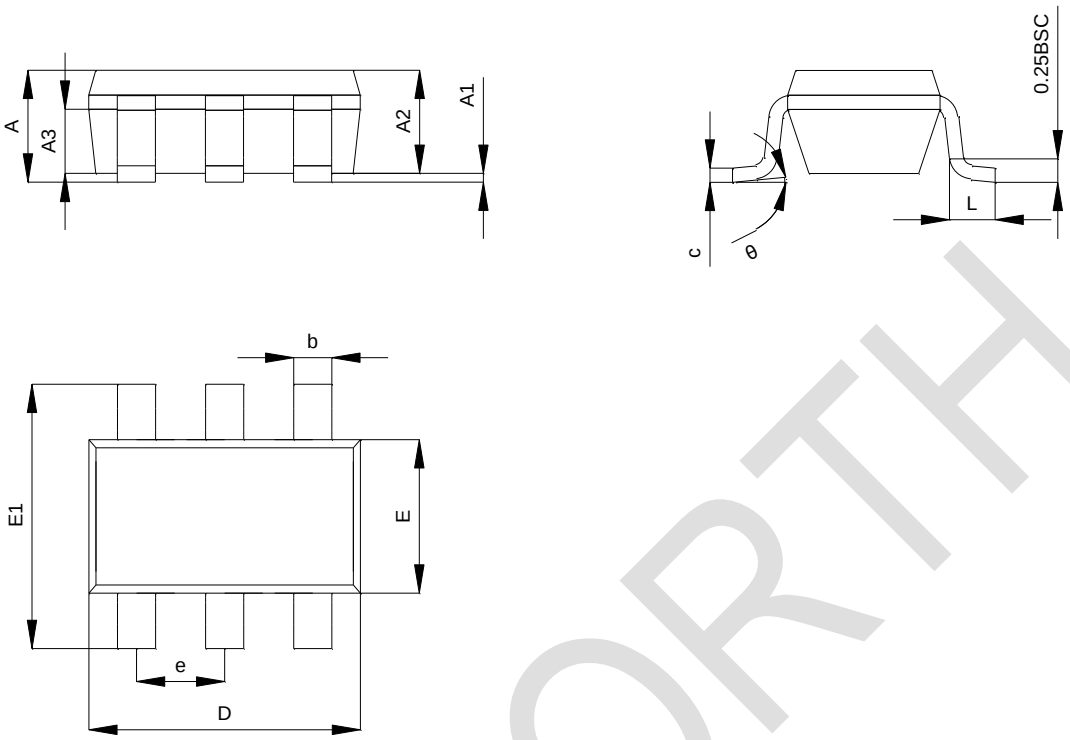


Output Short Circuit Protection



13 Package Information

SOT23-6L



Dimension / Symbol	Min(mm)	Nom(mm)	Max(mm)
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E	1.510	1.610	1.700
E1	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

14 Important Statement

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