1 Description

CN12039A/B/C/D is a highly performance AC/DC converter for wide voltage input, which integrates a PWM controller and 1200V MOSFET with high voltage startup to achieve ultra-low standby power consumption. CN12039A/B/C/D adopts hybrid PWM/PFM/Burst modulation technology which ensures optimal system efficiency over the full load range, and also integrates frequency dithering technology to simplify system EMI design. CN12039A/B/C/D provides excellent protection functions, including cycle-by-cycle overcurrent protection, CS resistor short-circuit protection, VDD over voltage protection, overload protection, output short-circuit protection, open feedback protection and over temperature protection.

2 Features

- Built-in 1200V MOSFET
- Built-in high-voltage starting circuit
- Built-in line voltage compensation and slope compensation
- Integrated frequency expansion technology
- Frequency tripling function to improve magnetic interference (Available in CN12039B/D)
- Integrated input undervoltage protection (Available in CN12039C/D)
- PWM/PFM/Burst hybrid control mode
- No-load power consumption <50mW @230 VAC
- Complete protection functions (OCP, OLP, UVLO, VDD OVP, OTP)

3 Applications

- Switching power supply
- Smart Meter

4 Ordering information

Product Code	Package	Quantity/Tape
CN12039AUFU	DIP-7	50/Tape
CN12039BUFU	DIP-7	50/Tape
CN12039CUFU	DIP-7	50/Tape
CN12039DUFU	DIP-7	50/Tape

5 Marking

Product Code	Marking
CN12039AUFU	CN12039A YYWW
CN12039BUFU	CN12039B YYWW
CN12039CUFU	CN12039C YYWW
CN12039DUFU	CN12039D YYWW

Note: YY=Year; WW=Week

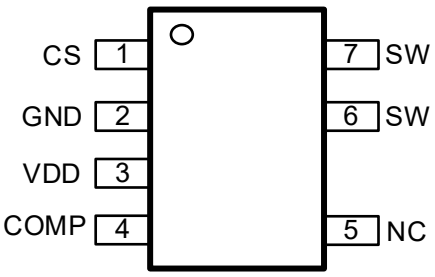
Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level (MSL): 3

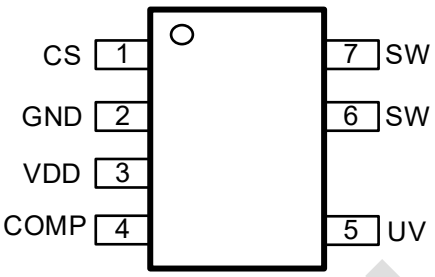
6 Model Description

Product Model	Function
CN12039A	No anti-magnetic function No input undervoltage protection
CN12039B	With anti-magnetic function No input undervoltage protection
CN12039C	No anti-magnetic function With input undervoltage protection
CN12039D	With anti-magnetic function With input undervoltage protection

7 Pinout

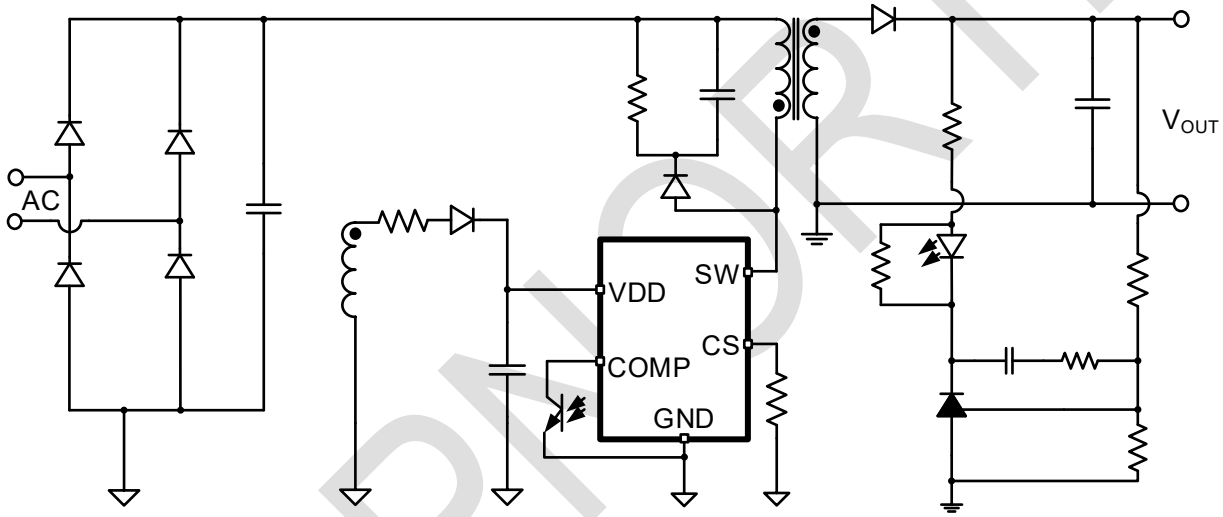


DIP-7
CN12039A、CN12039B

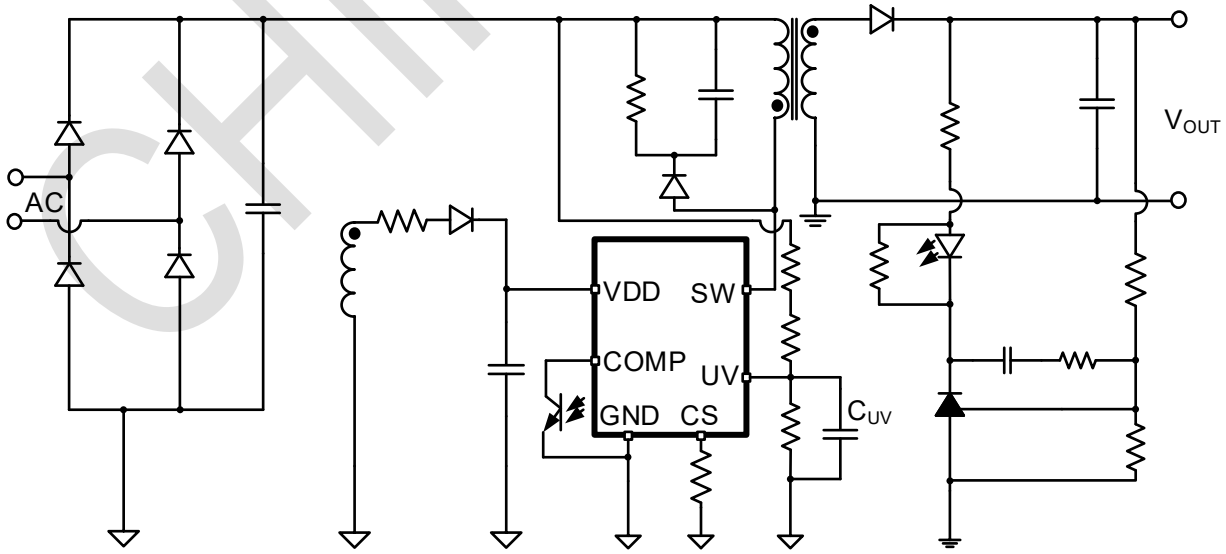


DIP-7
CN12039C、CN12039D

8 Typical Application



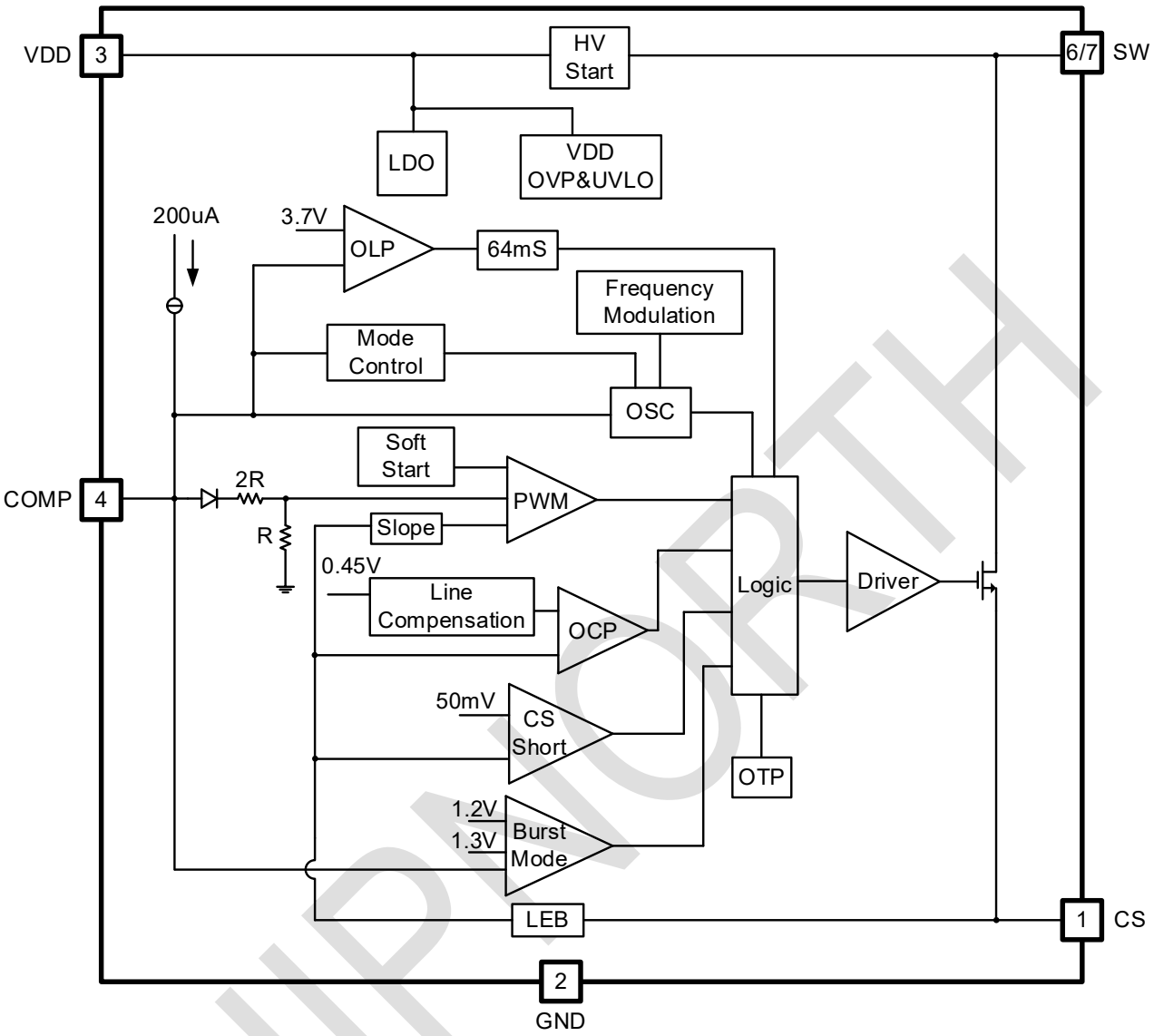
Typical Application Diagram of CN12039A, CN12039B



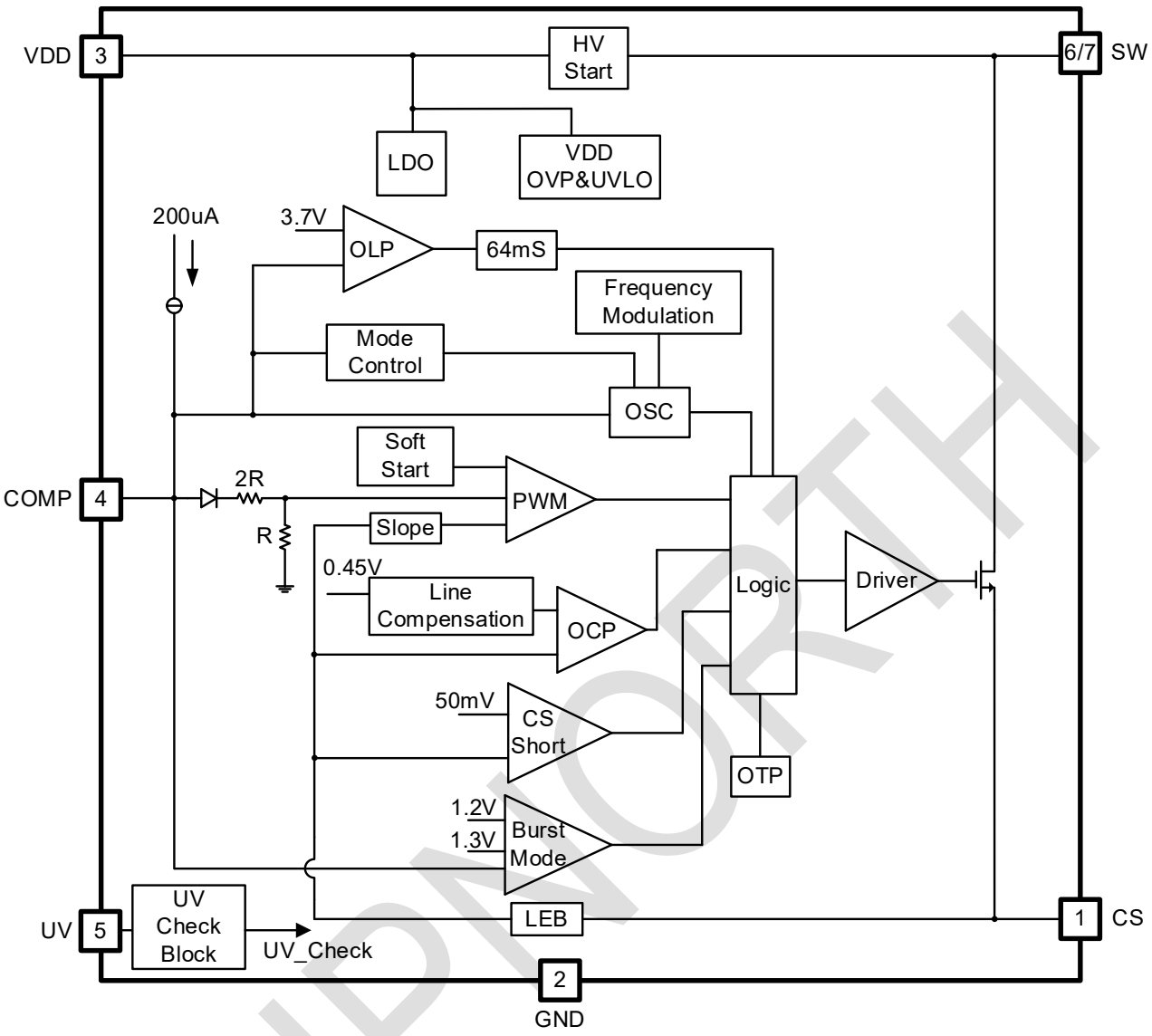
Typical Application Diagram of CN12039C, CN12039D

Note: The recommended C_{UV} value is about 10nF

9 Block Diagram



Functional Block Diagram of CN12039A, CN12039B



Functional Block Diagram of CN12039C, CN12039D

10 Pin Descriptions

Pin Name	Pin No.	Descriptions
CS	1	Built-in high voltage MOSFET source pin, current sense pin
GND	2	Ground
VDD	3	Operating voltage input pin
COMP	4	Feedback pin
NC/UV	5	NC: No connection (only available in CN12039A, CN12039B) UV: Input undervoltage protection detection pin (only available in CN12039C, CN12039D)
SW	6/7	Built-in high-voltage MOSFET drain pin, connected to transformer primary winding

11 Specifications

11.1 Absolute Maximum Ratings

Parameter	Value	Units
VDD pin withstand voltage	50	V
SW pin withstand voltage	1200	V
UV, CS, COMP pin withstand voltage	-0.3~5.5	V
Ambient temperature	-40~105	°C
Soldering Temperature	260（soldering,10s）	°C
Storage Temperature Range	-55~150	°C
Drain pulse current (Tpulse=100us)	2	A

Note: The limit parameter is a threshold that can't be exceeded under any condition (even an instant). Once the chip runs beyond the limit parameters, it may cause aging or permanent damage. The limit parameter only emphasizes numerical values and does not necessarily indicate that the chip can work properly under these limits.

11.2 ESD Ratings

Discharge mode	Standard	Value	Units
HBM	ANSI/ESDA/JEDEC JS-001-2023	±4000	V
CDM	ANSI/ESDA/JEDEC JS-002-2022	±2000	V

11.3 Typical Output Power

Package	Input Voltage Range	Open Average Power	Open Peak Power
DIP-7	85-425Vac	11W	14W
	230V±15%	13W	18W

11.4 Thermal Information

Parameter	Descriptions	Value	Unit
$R\theta_{JA}$	Junction to ambient	80	°C/W
$R\theta_{JC}$	Junction to case	40	°C/W

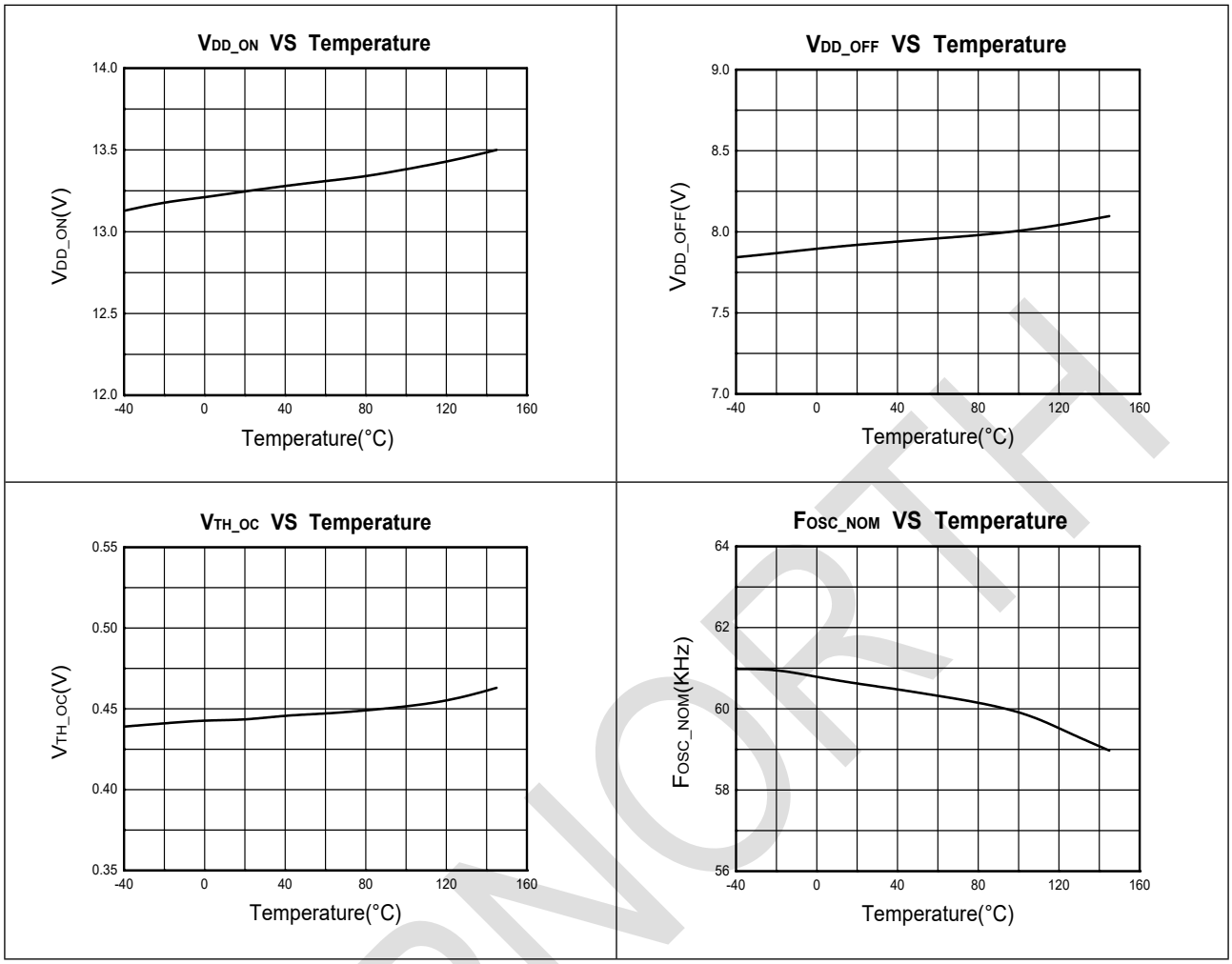
11.5 Electrical Characteristics

Test conditions: TA=25°C, VDD=15V, unless otherwise specified.

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Chip Power Supply Section						
Starting Voltage	V_{SW_START}				55	V
Startup Charging Current	I_{DD_CH}	V_{SW}=105V, V_{COMP}=GND, V_{DD}=10V		1.8		mA
Operating Voltage Range	V_{DD}	After turn-on	9		28	V
VDD Over-Voltage Protection	V_{DDOVP}	V_{CS}=0V, V_{COMP}=2V, Ramp up VDD until gate is off	28	30	32	V
UVLO Threshold Voltage	V_{DDON}	V_{COMP}=GND	12	13	14	V
	V_{DDOFF}	V_{COMP}=GND	7.5	8	8.5	V
Quiescent Current	I_{DD0}	V_{DD}=15V, V_{COMP}=GND		1	1.5	mA
Operating Current	I_{DD1}	V_{DD}=15V, V_{COMP}=2V		2	3	mA
Protection Mode Current	I_{DD_FAULT}			170	220	uA
Under-Voltage Working Current	I_{DD_OFF}	V_{DD}=6V		100	130	uA
COMP Section						
Open Loop Voltage	V_{COMP_OPEN}			4.8		V
Overload Protection Threshold	V_{COMP_OLP}			3.7		V
Anti-magnetic Mode Threshold (Available in CN12039B/D)	V_{COMP_TRI}			3.0		V
PFM Operating Mode Threshold	V_{COMP_PFM}	Voltage falling when frequency decrease		2.0		V
Burst Mode Threshold	V_{COMP_BM}	Voltage falling		1.2		V
Burst Mode Hysteresis Threshold	$V_{COMP\_BM\_HYS}$	Voltage rising		1.3		V
COMP Short Circuit Current	I_{COMP}	V_{COMP}=GND		-200		uA
Overload Protection Delay Time	T_{D_OLP}			64		mS
Detection Voltage Gain	A_{VCS}			3.3		V/V
Current Detection Section						
Soft Start Time	T_{SS}			10		mS
Minimum T_{ON}	T_{ON_MIN}			500		nS
Turn Off Delay Time	T_D			150		nS
Leading-Edge Blanking Time	T_{LEB}			350		nS
CS Limit Threshold	V_{TH_OC}		0.425	0.45	0.475	V
CS Clamp Voltage	$V_{OCP\_CLAMPING}$			0.55		V
Built-in Oscillator Section						
Maximum Switching Frequency (Available in CN12039B/D)	F_{OSC_MAX}		162	180	198	KHz
Switching Frequency	F_{OSC}	VDD in operating voltage range, V_{COMP}=2V	54	60	66	KHz
Frequency Jitter Range	F_D			±5		KHz
Modulation Frequency	F_M			250		Hz

Maximum Duty Cycle	D_{MAX}		70		85	%
Burst-Mode Frequency	F_{Burst}		21.5	25		KHz
UV Detection Section						
Pull-up current	I_{UV}			1		uA
Clamp Voltage	V_{UV_CLP}	$I_{\_UV}$=0.5mA	3.9	4.5	5.1	V
Detection Threshold Voltage	V_{UV_REF}		0.52	0.55	0.58	V
Over-Temperature Protection Section						
Over-Temperature Protection	T_{SD}		135	150		°C
Over-Temperature Protection Hysteresis	T_{HYST}			30		°C
Built-In MOSFET Section						
Drain-Source Breakdown Voltage	BV_{DSS}	I_{SW}=250uA, T_J=25°C	1200			V
MOSFET On-Resistance	R_{DS_ON}	I_{SW}=0.5A, T_J=25°C		9		Ω

11.6 Characteristic Curve



12 Detailed Description

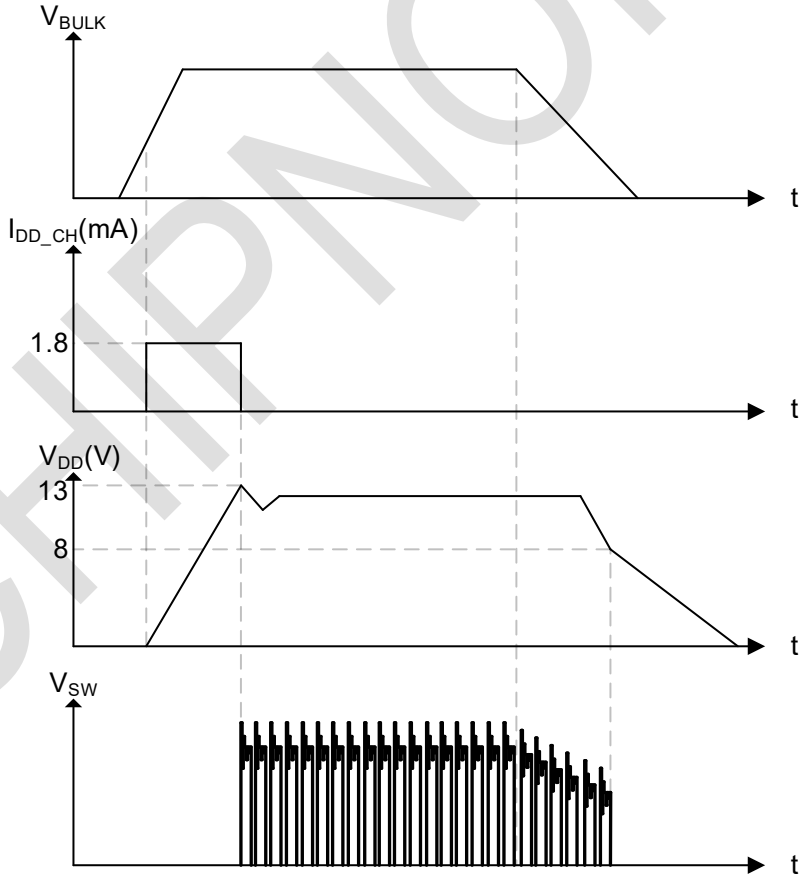
12.1 Overview

CN12039A/B/C/D is an efficient switching power supply controller integrating power MOSFET and PWM controller, and the extremely compact peripheral components make it easier to design switching power supplies. CN12039A/B/C/D provides extremely complete and intelligent protection functions, including cycle-by-cycle overload protection, over-voltage protection, CS resistor short circuit protection, over-temperature protection and soft-start function, etc. In addition, the hybrid modulation technique of PWM, PFM and Burst can realize the best performance of the system under different loads; and the unique high-voltage start-up design can realize lower standby power consumption. The built-in frequency dithering function and frequency modulation technology enable better EMI performance, and the CN12039A/B/C/D provides a reliable solution for ultra-low standby power applications.

12.2 Functional Description

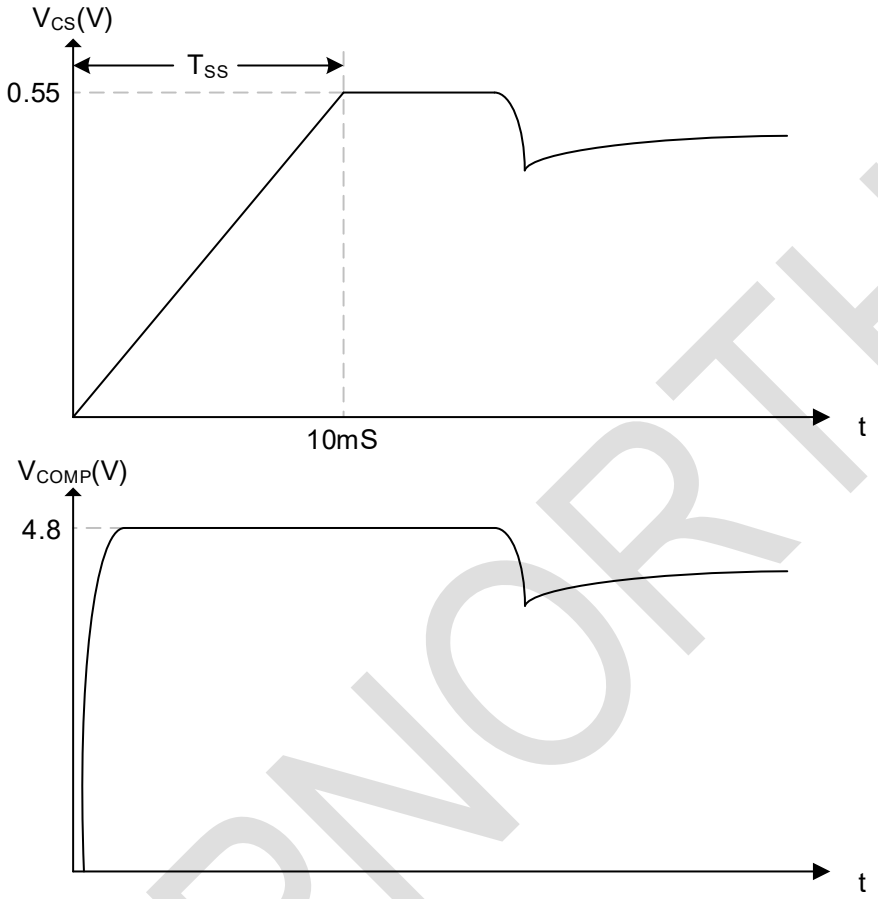
12.2.1 Startup

The built-in high voltage starter MOS provides 1.8 mA current to charge the external VDD capacitor. Once the VDD voltage reaches 13V, CN12039A/B/C/D starts to work immediately, at this time the high voltage starter MOS will stop charging the VDD capacitor, the VDD capacitor discharges to maintain the chip working, the VDD voltage drops slightly, then the transformer auxiliary winding provides energy to the VDD capacitor to keep the VDD capacitor voltage stable.



12.2.2 Soft Start

During the start-up phase, the limit value of the maximum peak current at the drain of the built-in power MOS is slowly raised; this minimizes the stress on the device and prevents transformer saturation. The soft-start time of CN12039A/B/C/D is typically 10ms.



12.2.3 Output Driver

CN12039A/B/C/D adopts unique driving technology and optimizes the totem pole structure to reasonably configure the driving current and dead time, resulting in better EMI performance and lower loss.

12.2.4 Oscillator

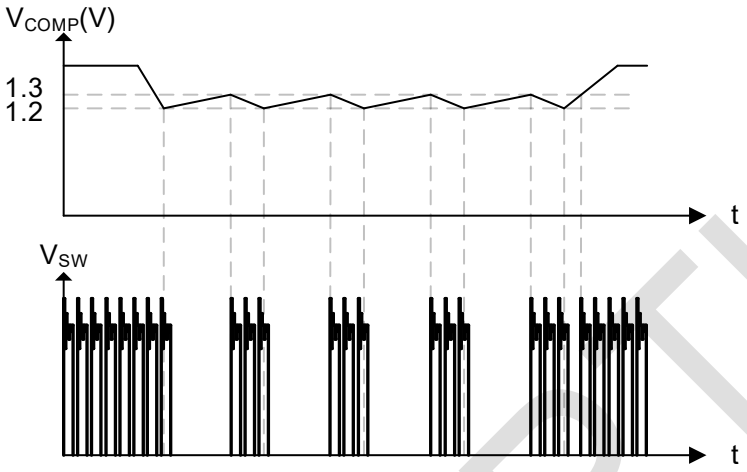
CN12039A/B/C/D does not require peripheral circuitry for frequency setting, the built-in oscillator frequency is fixed at 60KHz, equipped with a unique frequency dithering technology, which can further optimize the EMI characteristics.

12.2.5 Feedback Control

The chip adopts the current mode control technology, the voltage of COMP pin can control the current of the power MOS, so as to achieve the purpose of voltage regulation.

12.2.6 Burst Operation Mode

Under light load, CN12039A/B/C/D will operate in Burst mode to reduce system power consumption. When the load is lightened, the COMP pin voltage decreases and the chip enters the Burst operation mode when V_{COMP} is less than the Burst mode threshold (typically 1.2V). Once V_{COMP} exceeds the Burst mode hysteresis threshold, CN12039A/B/C/D can exit Burst mode.



12.2.7 PFM Operation Mode

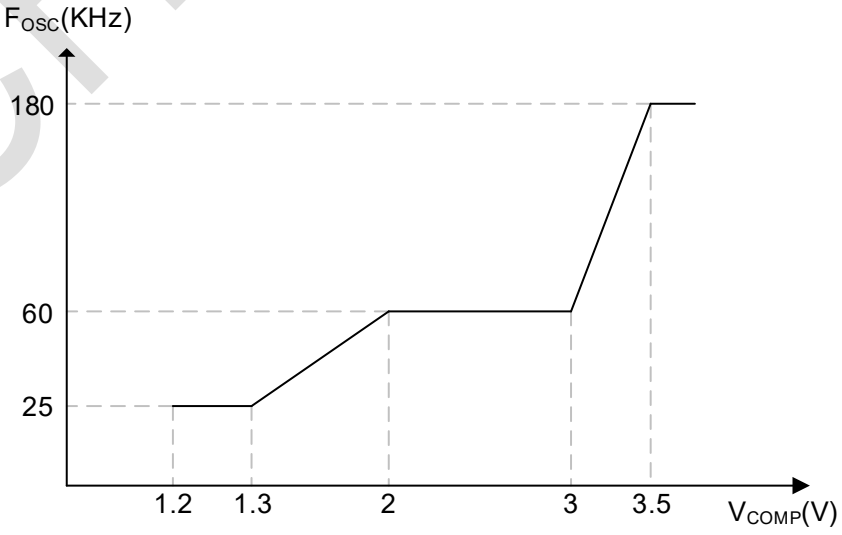
CN12039A/B/C/D provides a PFM operation mode, which detects the COMP pin voltage and reduces the switching frequency under light load and no-load conditions to improve the light load efficiency. When the COMP pin voltage is less than 2V, the chip enters the PFM operation mode, and the minimum frequency of this chip is 25KHz, where the switching frequency decreases with the load, to eliminate noise under light load conditions.

12.2.8 PWM Operation Mode

When CN12039A/B/C/D operates in the heavy load V_{COMP} greater than 2V condition, it enters the PWM operation mode and the operating frequency is kept constant at 60KHz.

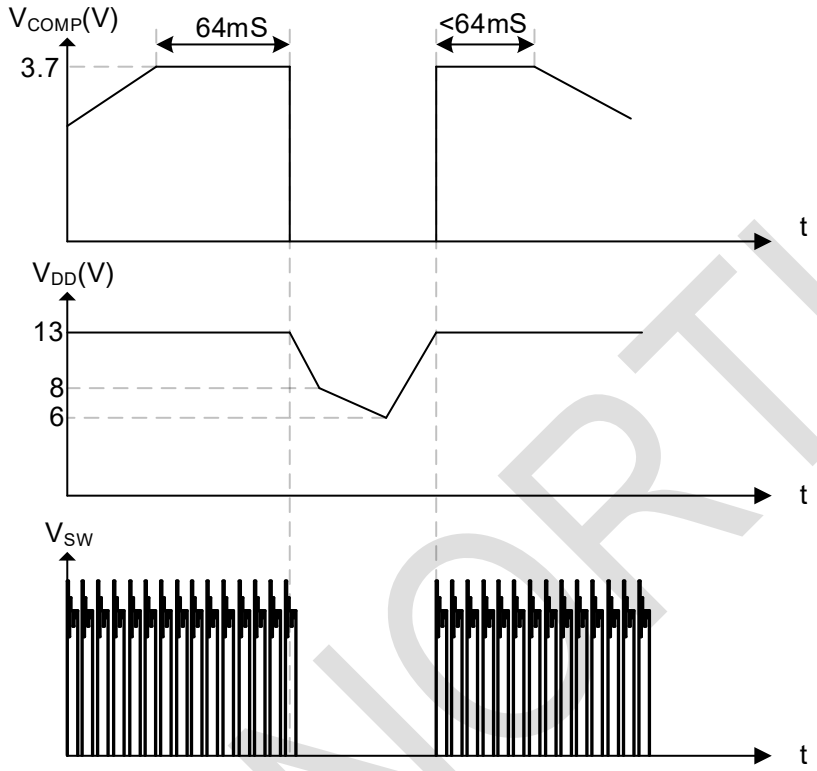
12.2.9 Frequency Ascension Mode (Available in CN12039B/D)

When CN12039B/D operates under strong magnetic or overload V_{COMP} greater than 3V, it will enter the frequency ascension mode, and the operating frequency will be linearly increased to 3 times of the original with V_{COMP} to compensate for the effect of the transformer inductance decreasing under the strong magnetic field.



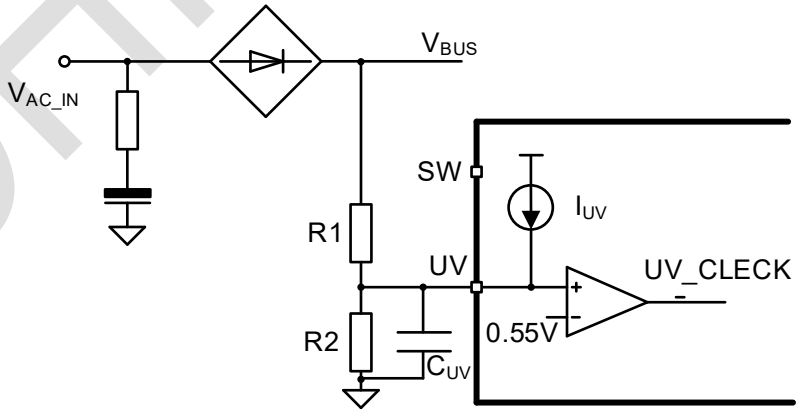
12.2.10 Overload Protection

When the load current exceeds the preset value, the system will enter the overload protection ("hiccup" type protection): it can protect the system under abnormal conditions. When the V_{COMP} pin voltage exceeds 3.7V and after a fixed delay of 64ms, the chip will enter the overload protection, and after the fault is removed, the chip can resume operation.



12.2.11 Input undervoltage protection (Available in CN12039C/D)

CN12039C/D integrates an input voltage detection module, from the input filter capacitor, through the voltage divider resistor connected to UV pin, the system will detect the UV voltage after startup and compare it with the internal reference, when the UV voltage is greater than 0.55V, the system will start to work, if UV voltage is lower than 0.55V, it will stop working. UV pin needs to be connected to a filter capacitor of 10nF to attenuate the coupling interference of the SW pin to UV pin.



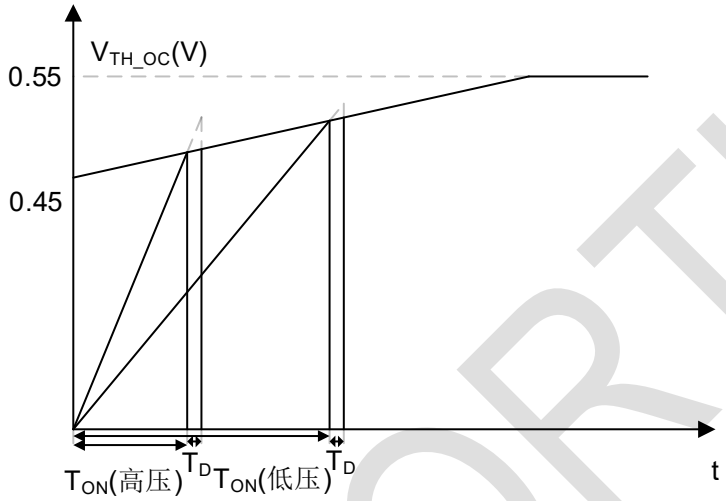
The input starting voltage V_{AC_IN} is calculated as follows:

$$V_{AC\_IN} = \frac{1}{1.414} \times \left(\frac{0.55}{R2} - I_{UV}\right) \times (R1 + R2)$$

R1 and R2 are in KΩ and I_{UV} is in mA.

12.2.12 Line Voltage Compensation

CN12039A/B/C/D provides overcurrent line voltage compensation to achieve constant output power limitation over the full voltage range.T_D is the conduction delay time. Under high voltage conditions, the turn-on time is shorter compared to low voltage conditions. After line voltage compensation, the VTH_OC is lower during high voltage input, but the current sampling value at the CS pin during the TD period is higher. These two factors collectively result in a consistent peak current level under both high and low voltage inputs



12.2.13 Ramp Compensation

CN12039A/B/C/D provides ramp compensation, which superimposes a voltage sawtooth signal on the sampled current signal and is used to improve the stability of the system loop.

12.2.14 Overcurrent Protection

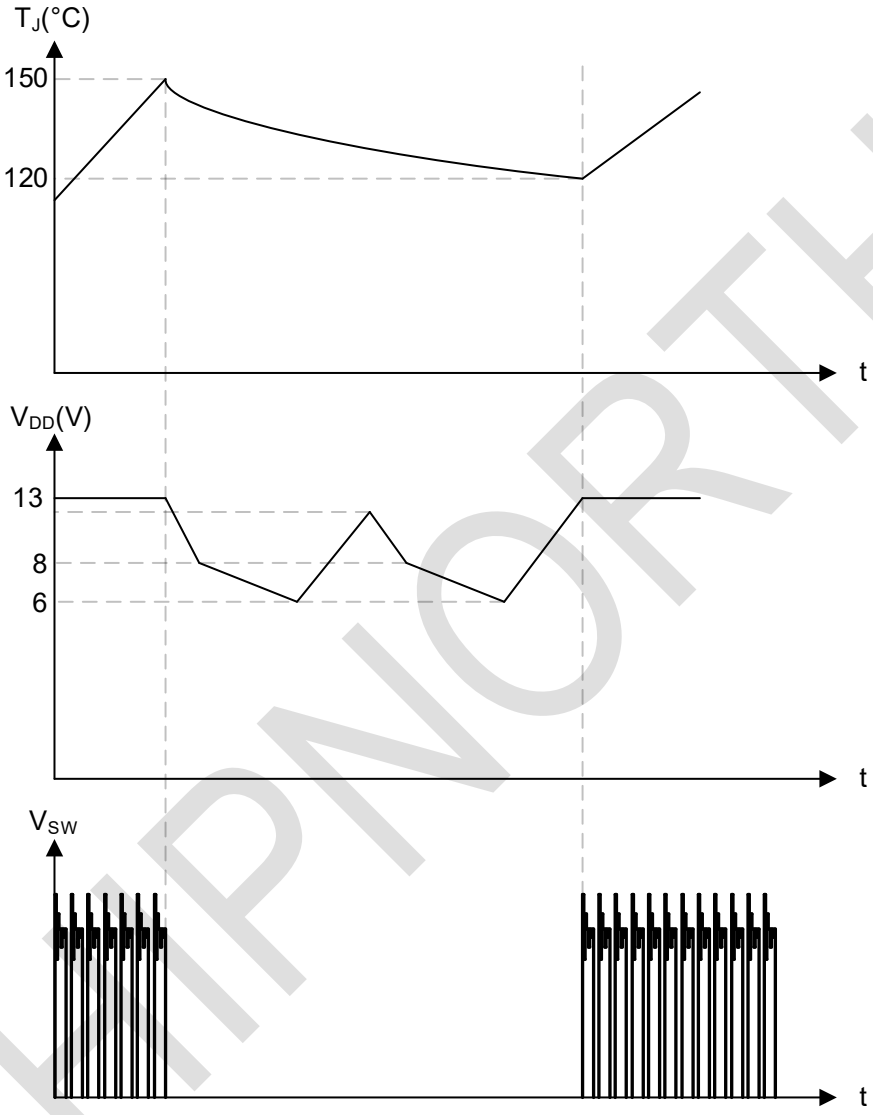
CN12039A/B/C/D has cycle-by-cycle overcurrent protection. The current flowing through MOSFET can be detected and controlled by setting the resistor between the CS pin and GND to adjust the overcurrent protection value.

12.2.15 CS Resistor Short Circuit Protection

CN12039A/B/C/D provides CS resistor short circuit protection. If the CS resistor is short-circuited before the system starts up, the chip enters the CS resistor short-circuit protection state. It can protect the system under abnormal conditions.

12.2.16 Over Temperature Protection

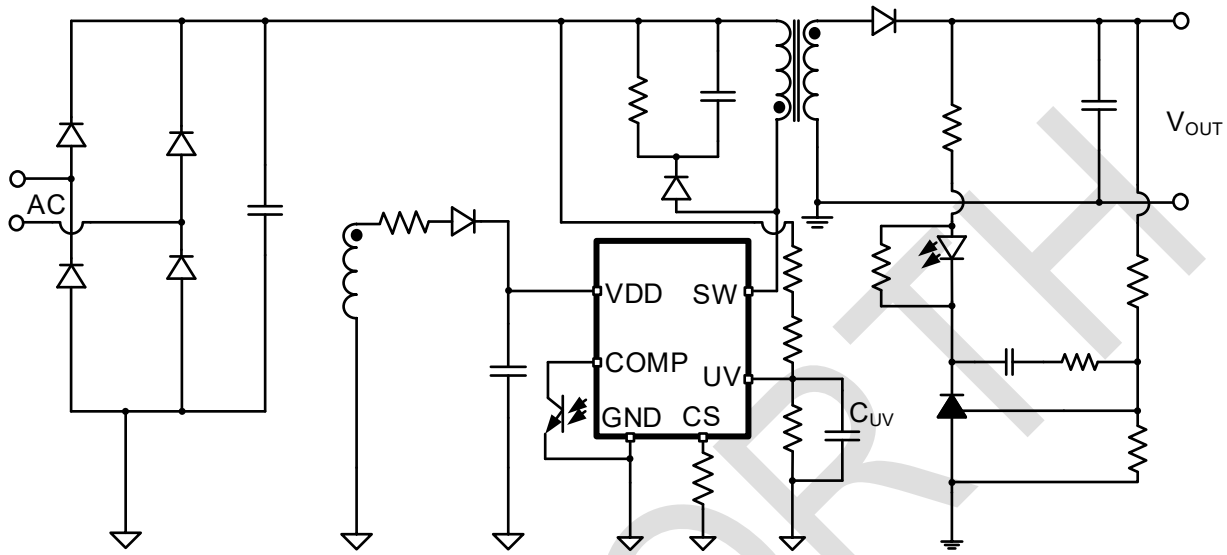
The power MOSFET and the control circuit are integrated together, making it easier for the control circuit to detect the temperature of the MOSFET. When the temperature exceeds 150°C, the chip enters the over-temperature protection state; when the temperature recovers to 120°C, the chip can resume operation.



13 Application Information

13.1 Typical Application

The following figure shows the schematic of a typical application circuit that can be used as a means of evaluating the performance of CN12039A/B/C/D. This section describes the design process specific to the application schematic.



13.2 Selection of Input Capacitor

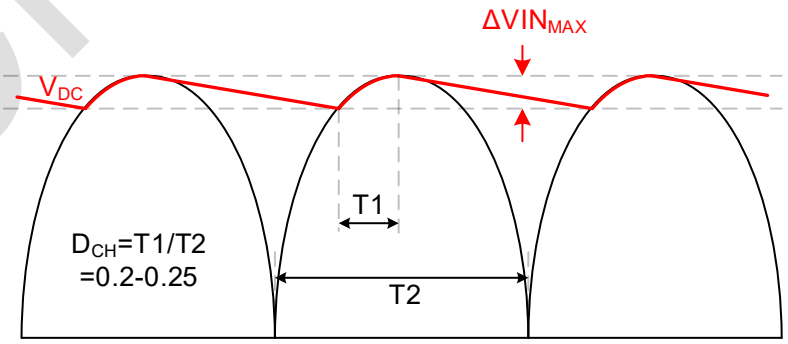
$$C_{BUS} = \frac{P_{IN} \times (1 - D_{CH})}{\sqrt{2} \times VAC_{MIN} \times 2 \times f_L \times \Delta VIN_{MAX}}$$

- Input Power $P_{IN}=P_O/\eta$ (η is the efficiency)
- VAC_{MIN} is the minimum AC input voltage
- f_L is the line AC frequency, generally 50~60Hz
- D_{CH} is the duty cycle, its typical value is 0.2~0.3

General ΔVIN_{MAX} is set as 10%~30% of $\sqrt{2}VAC_{MIN}$.

Capacitor withstand voltage should be more than $VIN_{MAX} = \sqrt{2} \times VAC_{MAX}$, VAC_{MAX} is the maximum AC input voltage.

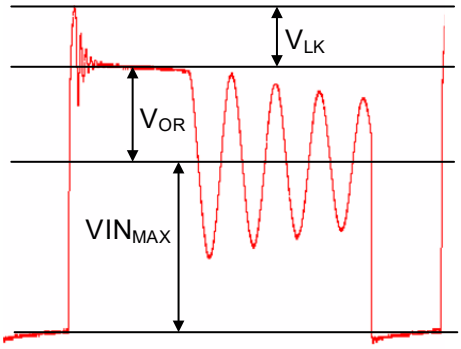
It is also possible to follow the values of 2~3uF/W for C_{BUS} at 85VAC~265VAC and 1uF/W for C_{BUS} at 195VAC~265VAC.



13.3 Transformer Design

13.3.1 Turns Ratio

When the MOSFET is turned off, the drain leakage inductance spike voltage V_{LK}, the input voltage VIN, and the output voltage V_{OR} reflected to the primary will be applied to DS of the MOSFET.



The reflected voltage V_{OR} is:

$$V_{OR} = V_{DS\_MAX} - V_{LK} - VIN_{MAX} - V_{MARGIN}$$

- V_{LK} is the leakage inductance spike voltage
- V_{DS_MAX} is the maximum MOSFET voltage
- V_{MARGIN} is the margin (100V for consumer, 300V for power)

From this, the turns ratio n can be calculated:

$$n = \frac{V_{OR}}{V_O + V_F}$$

- V_F is the output diode forward voltage drop

13.3.2 Maximum Duty Cycle

$$D = \frac{V_{OR}}{V_{OR} + VIN_{MIN}}$$

- VIN_{MIN} is the DC voltage corresponding to the lowest AC input voltage

$$VIN_{MIN} = (0.7\sim0.9) \times \sqrt{2} \times VAC_{MIN}$$

Note: The maximum duty cycle D should not exceed the maximum duty cycle of the chip, and to leave some margin, it is recommended to be around 0.5.

13.3.3 Peak Switching Current

The average input current I_{IN} is calculated from the output power and the preset efficiency:

$$I_{IN} = \frac{P_O}{\eta \times VIN_{MIN}}$$

The primary inductor current ramp center value I_L is:

$$I_L = \frac{I_{IN}}{D}$$

The peak switching current I_{PK} is:

$$I_{PK} = (1 + \frac{r}{2}) \times I_L$$

$$r = \frac{\Delta I}{I_L}$$

Where “r” is the current ripple rate, it is recommended that “r” be taken as 1, and ΔI is the variation of the primary inductor current.

13.3.4 Primary-Side Inductance Value

$$L_P = \frac{VIN_{MIN} \times D}{I_L \times r \times F_{SW}}$$

Where F_{SW} is the switching frequency, and the typical value of the switching frequency of CN12039A/B/C/D is 60KHz.

13.3.5 Number of Winding Turns

Primary-side windings N_P:

$$N_P = \frac{I_{PK} \times L_P}{B_{PK} \times A_e}$$

- Where B_{PK} is the maximum magnetic flux density at full load

$I_{PK} = I_L + 0.5 \times I_L \times r$ at full load, $I_{PK} = 1.2 \times I_L + 0.5 \times I_L \times r$ at 120% load.

$$\frac{B_{PK}}{B_{MAX}} = \frac{1 + 0.5 \times r}{1.2 + 0.5 \times r}$$

The flux density B_{MAX} at 120% load is recommended not to exceed 0.35T, then the full load B_{PK} is not to exceed 0.31T when "r" is taken to be 1.

The effective cross-sectional area Ae of the core is obtained by selecting a suitable core according to the output power.

The number of turns N_S of the secondary-side winding can be obtained as:

$$N_S = \frac{N_P}{n}$$

The VDD voltage range is 9V to 28V, taking the value of 15V at full load, and the number of turns of the auxiliary winding N_A:

$$N_A = N_S \times \frac{VDD + V_F}{V_O + V_F}$$

Where V_F is the rectifier diode forward conduction drop voltage

13.3.6 Calculation of Primary and Secondary Wire Diameters

The primary coil current RMS value I_{P_RMS} is:

$$I_{P\_RMS} = I_L \times \sqrt{\frac{D}{3} \times (3 + \frac{r^2}{4})}$$

The secondary coil current RMS value I_{S_RMS} is:

$$I_{S\_RMS} = n \times I_L \times \sqrt{\frac{1 - D}{3} \times (3 + \frac{r^2}{4})}$$

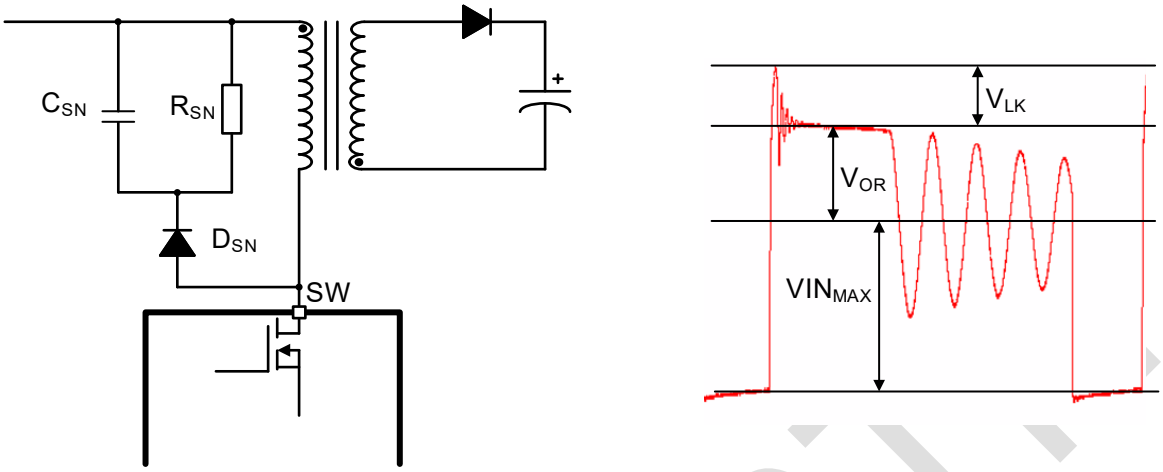
The cross-sectional area of the winding wire $S = I_{RMS}/J$, where "J" is the current density, generally taken as 6~8A/mm^2.

The winding wire diameter d is

$$d = \sqrt{\frac{4 \times S}{\pi}}$$

13.4 RCD Design

The following figure shows the reference diagram of the RCD absorption circuit with the V_{DS} waveform on the right.



In the right figure, V_{LK} is the leakage inductance spike voltage, V_{OR} is the transformer reflection voltage, the diode in the RCD circuit is recommended to choose a high voltage diode with a current capacity of 1A or more, and the capacitor is selected by the following formula:

$$P_{SN} = 0.5 \times L_{LK} \times I_{PK}^2 \times F_{SW} \times \frac{V_{LK} + V_{OR}}{V_{LK}}$$

$$R_{SN} = \frac{(V_{LK} + V_{OR}) \times V_{LK}}{0.5 \times L_{LK} \times I_{PK}^2 \times F_{SW}}$$

$$C_{SN} = \frac{V_{LK} + V_{OR}}{R_{SN} \times F_{SW} \times \Delta V_{SN}}$$

Among them:

- P_{SN} is the leakage inductance loss
- L_{LK} is the transformer leakage inductance
- I_{PK} is the transformer peak current
- F_{SW} is the switching frequency, typical value is 60KHz
- ΔV_{SN} is the capacitor ripple, according to experience, the value is generally taken as 10%~30% of the capacitor voltage.

13.5 Selection of CS Resistance

The CS pin is the source of the internal integrated MOSFET. The CN12039A/B/C/D has cycle-by-cycle overcurrent protection with V_{CS}=0.45V, and the peak current can be detected and controlled by the CS-to-ground resistor R_{CS}. Calculate the R_{CS} according to the following formula.

$$R_{CS} = \frac{V_{CS}}{I_{PK}}$$

13.6 Selection of VDD Capacitor

VDD capacitor in the chip startup stage, the VDD capacitor is first charged through built-in high voltage starter MOS, and then discharge to maintain chip operation, so the choice of VDD capacitor directly affects the startup time, it is recommended 10uF ~ 47uF, the calculation formula is as follows:

$$T_{START} = \frac{C_{VDD} \times VDD}{I_{DD\_CH}}$$

For example, if the VDD capacitance is selected to be 22uF, I_{DD_CH} =1.8mA, and the startup voltage threshold of CN12039A/B/C/D is 13V, the startup time is T_{START}=159mS.

13.7 Selection of Output Rectifier Diode

The maximum reverse voltage V_{DR} of the output rectifier diode and the current RMS value I_{D_RMS} are:

$$V_{DR} = V_O + \frac{VIN_{MAX}}{n}$$

$$I_{D\_RMS} = I_{S\_RMS} \times \sqrt{\frac{VIN_{MIN}}{V_{OR}}}$$

In practice, the maximum reverse voltage V_{RRM} and the average forward current I_F of the rectifier diode are margined as follows:

$$V_{RRM} > 1.3 \times V_{DR}$$

$$I_F > 1.5 \times I_{D\_RMS}$$

13.8 Selection of Output Capacitor

The selection of the output capacitor mainly considers the RMS value of the ripple current, ESR and withstand voltage.

The ripple current I_{C_RMS} of the output capacitor is:

$$I_{C\_RMS} = \sqrt{(I_{D\_RMS})^2 - (I_O)^2}$$

The voltage ripple of the output capacitor is mainly caused by the charging and discharging of the capacitor and ESR.

The ripple caused by the charging and discharging of the capacitor is:

$$\Delta V_{CO} = \frac{I_O \times D}{C_O \times F_{SW}}$$

- C_O is the capacitance value

The ripple due to ESR is:

$$\Delta V_{ESR} = I_{PK} \times n \times R_{ESR}$$

- R_{ESR} is the ESR of the output capacitor

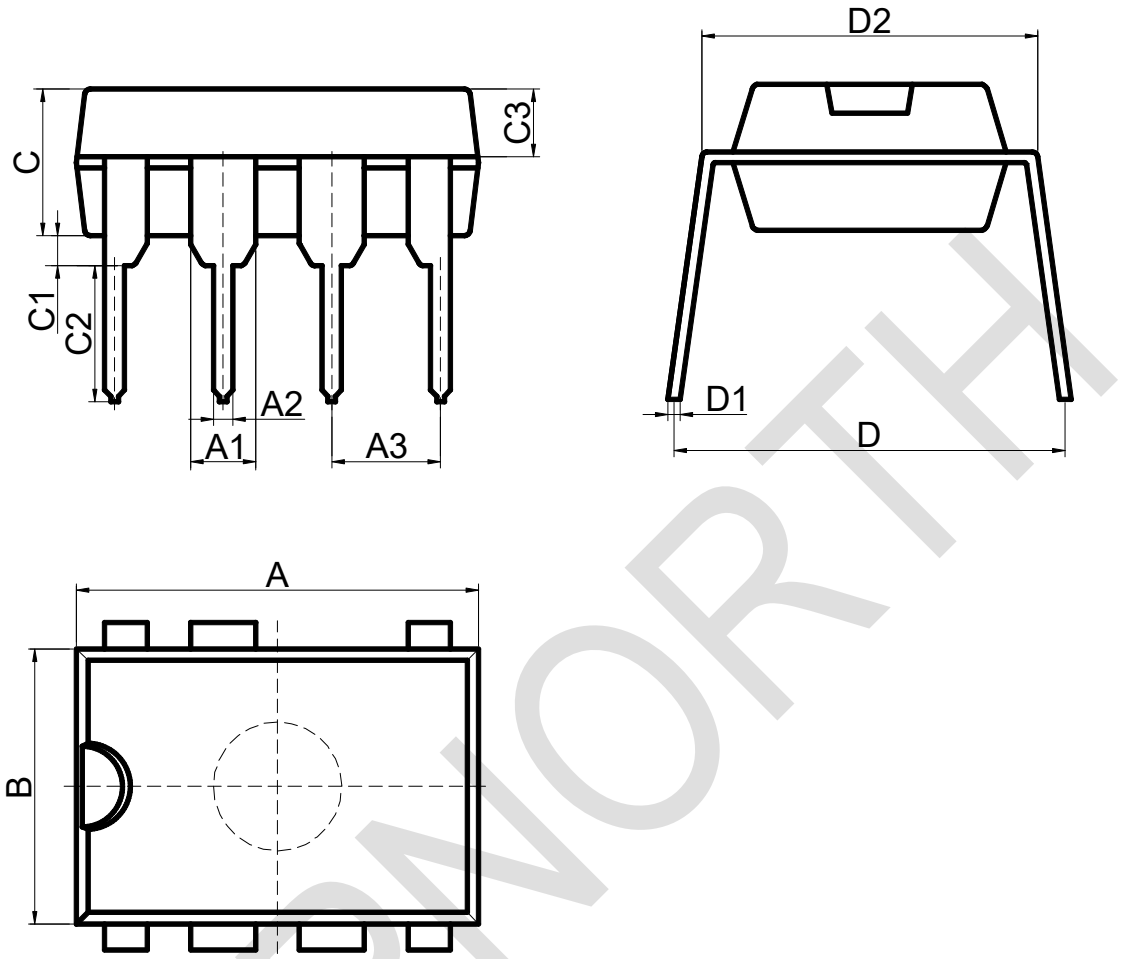
Since the electrolytic capacitor capacity is relatively large, the ripple due to ESR is mainly considered and R_{ESR} is calculated:

$$R_{ESR} = \frac{I_{PK} \times n}{\Delta V_{ESR}}$$

The withstand voltage of the output capacitor leaves a margin of at least 20% over the output voltage.

14 Package Information

DIP-7



Dimension / Symbol	Min(mm)	Nom(mm)	Max(mm)
A	9.15	9.25	9.35
A1		1.52REF	
A2	0.44	-	0.52
A3		2.54BSC	
B	6.25	6.35	6.45
C	3.2	3.3	3.4
C1	0.51	-	-
C2	3	-	-
C3	1.55	1.6	1.65
D	7.62	-	9.3
D1	0.25	-	0.29
D2		7.62REF	

15 Important Statement

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