1 Features

- Fixed 1/4 duty mode, 1/3bias voltages supporting a maximum of 160 segments
- Low power consumption design, 6uA current at typical condition
- Incorporates an internal OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Includes an I2C interface
- Compatible with TTL/CMOS
- High EMC immunity

2 Applications

- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

3 Ordering information

Product Number	Package	Quantity/Tape
CN90C4S40	TSSOP48	2500/Reel

4 Marking

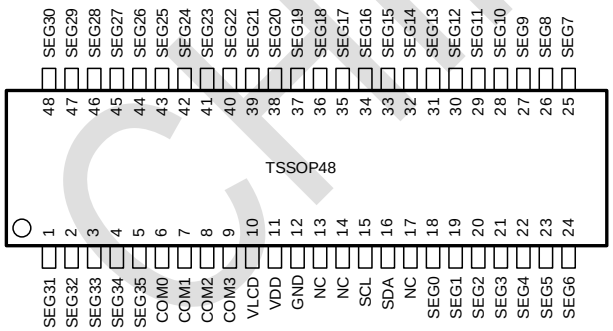
Product Number	Marking
CN90C4S40	CN90C4S40 YYWWAS XXXXXXXX

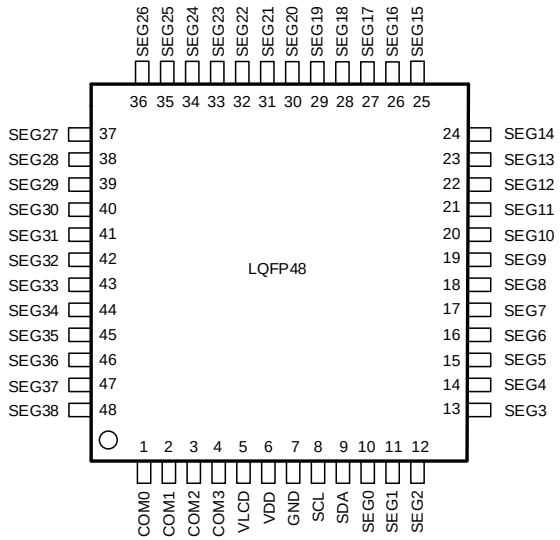
Note: YY=Year WW=Week AS=Factory code XXXXXXXX=Wafer lot number

Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

5 Pinout

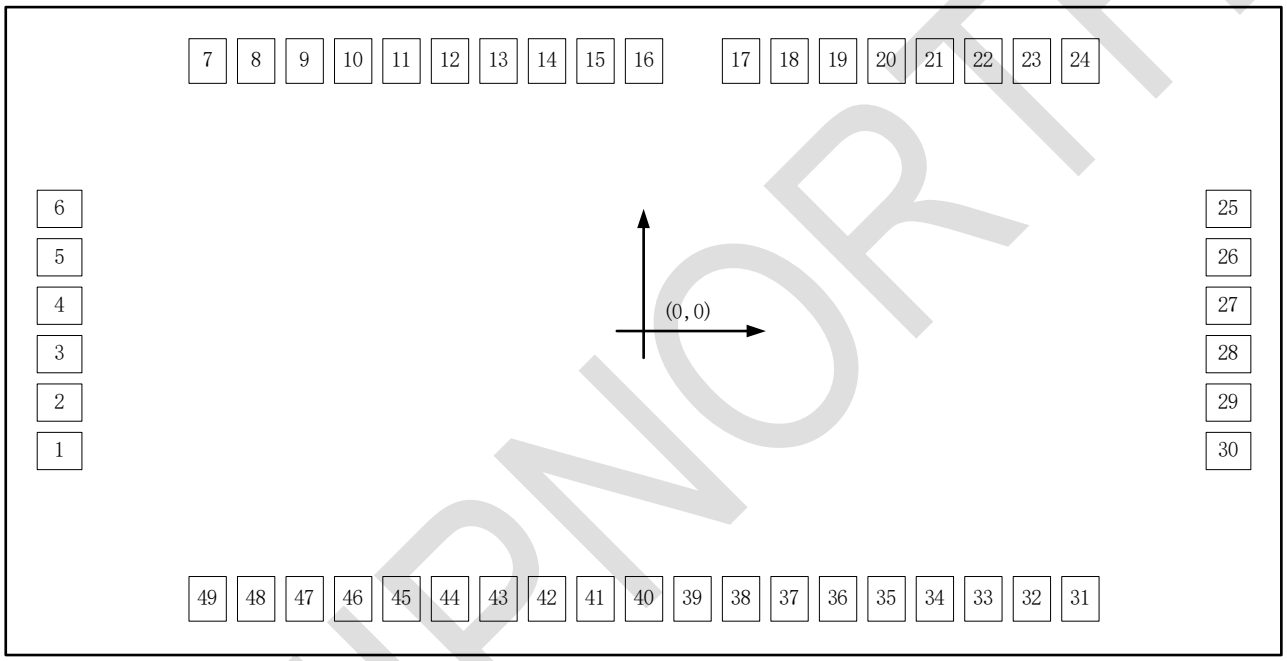




6 Pin Descriptions

Pin Name	I/O	TSSOP48	LQFP48	Function
SDA	I/O	16	9	2-line serial data input and output
SCL	I	15	8	2-line serial clock input
VSS	I	12	7	Connect to GND
VDD	I	11	6	Power supply for logic
VLCD	I	10	5	The default LCD drive voltage is set to a low level
SEG0~35	O	18~48,1~5		SEGMENT driver output for LCD
SEG0~38	O		10~48	SEGMENT driver output for LCD
COM0~3	O	6~9	1~4	COMMON driver output for LCD

7 PAD Assignment for COB

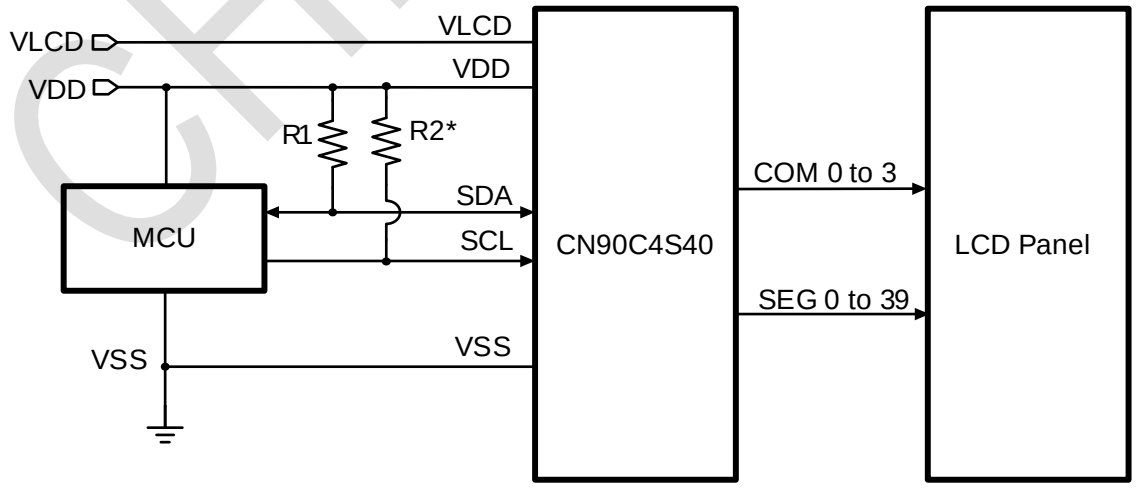


8 PAD Coordinates for COB

UNIT： μm

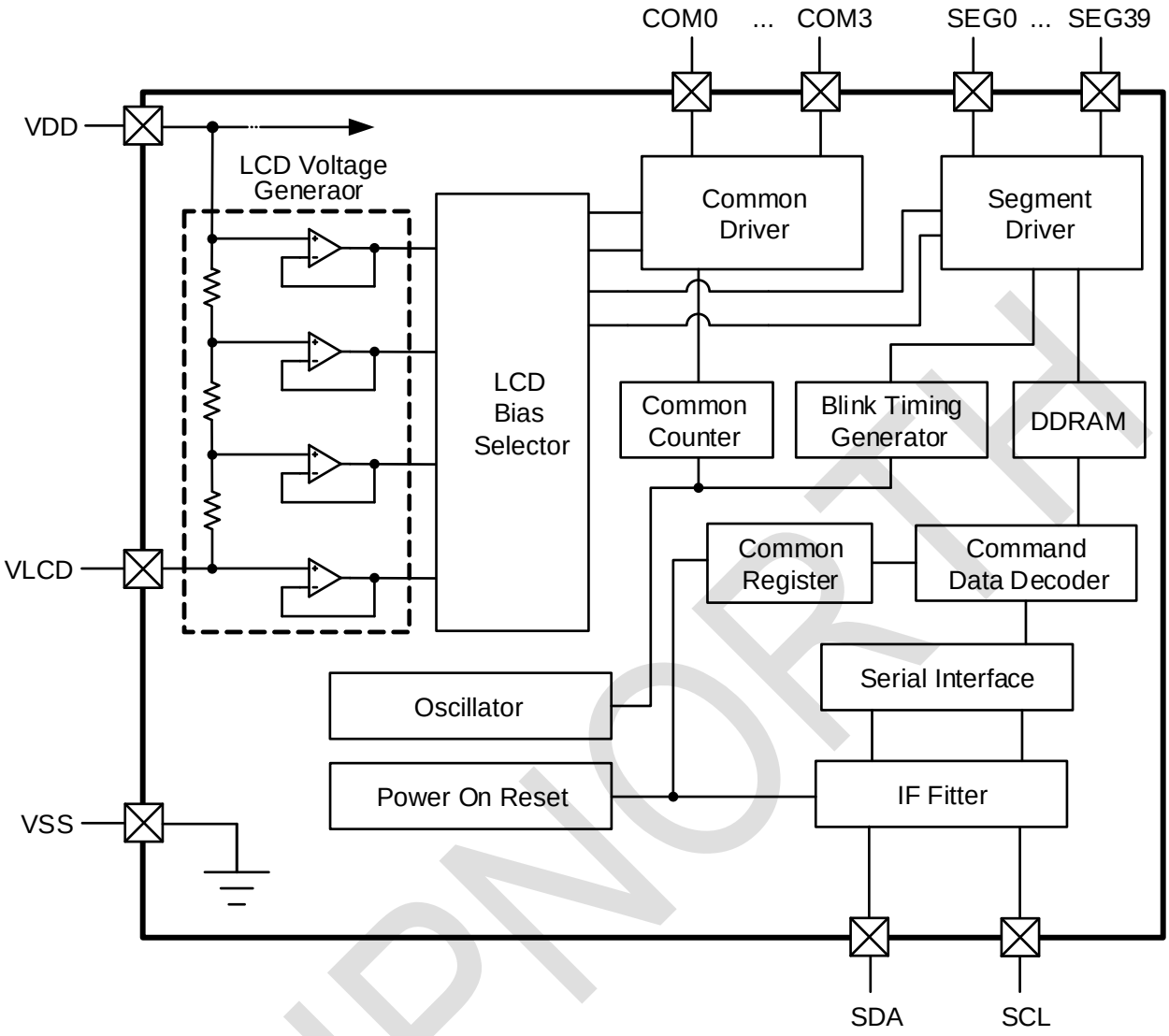
No	Name	X	Y	Size	No	Name	X	Y	Size
1	SEG33	-783	-161	60x50	26	SEG8	784	99	60x50
2	SEG32	-783	-96	60x50	27	SEG7	784	34	60x50
3	SEG31	-783	-31	60x50	28	SEG6	784	-31	60x50
4	SEG30	-783	34	60x50	29	SEG5	784	-96	60x50
5	SEG29	-783	99	60x50	30	SEG4	784	-161	60x50
6	SEG28	-783	164	60x50	31	SEG3	585.5	-359.5	50x60
7	SEG27	-584.5	362.5	50x60	32	SEG2	520.5	-359.5	50x60
8	SEG26	-519.5	362.5	50x60	33	SEG1	455.5	-359.5	50x60
9	SEG25	-454.5	362.5	50x60	34	SEG0	390.5	-359.5	50x60
10	SEG24	-389.5	362.5	50x60	35	SDA	325.5	-359.5	50x60
11	SEG23	-324.5	362.5	50x60	36	SCL	260.5	-359.5	50x60
12	SEG22	-259.5	362.5	50x60	37	GND	195.5	-359.5	50x60
13	SEG21	-194.5	362.5	50x60	38	VDD	130.5	-359.5	50x60
14	SEG20	-129.5	362.5	50x60	39	VLCD	65.5	-359.5	50x60
15	SEG19	-64.5	362.5	50x60	40	COM3	0.5	-359.5	50x60
16	SEG18	0.5	362.5	50x60	41	COM2	-64.5	-359.5	50x60
17	SEG17	130.5	362.5	50x60	42	COM1	-129.5	-359.5	50x60
18	SEG16	195.5	362.5	50x60	43	COM0	-194.5	-359.5	50x60
19	SEG15	260.5	362.5	50x60	44	SEG39	-259.5	-359.5	50x60
20	SEG14	325.5	362.5	50x60	45	SEG38	-324.5	-359.5	50x60
21	SEG13	390.5	362.5	50x60	46	SEG37	-389.5	-359.5	50x60
22	SEG12	455.5	362.5	50x60	47	SEG36	-454.5	-359.5	50x60
23	SEG11	520.5	362.5	50x60	48	SEG35	-519.5	-359.5	50x60
24	SEG10	585.5	362.5	50x60	49	SEG34	-584.5	-359.5	50x60
25	SEG9	784	164	60x50					

9 Typical Application



Note: * R2 is optional.

10 Block Diagram



11 Specifications

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3 to +6.5	V	Power supply
Power Supply Voltage1	V_{LCD}	-0.3 to V_{DD}	V	LCD drive voltage
Input voltage range	V_{IN}	-0.3 to VDD+0.3	V	
Soldering Temperature	T_{lead}	260（soldering,10s）	°C	
Operational temperature range	T_{opr}	-40 to +105	°C	
Storage temperature range	T_{stg}	-55 to +150	°C	

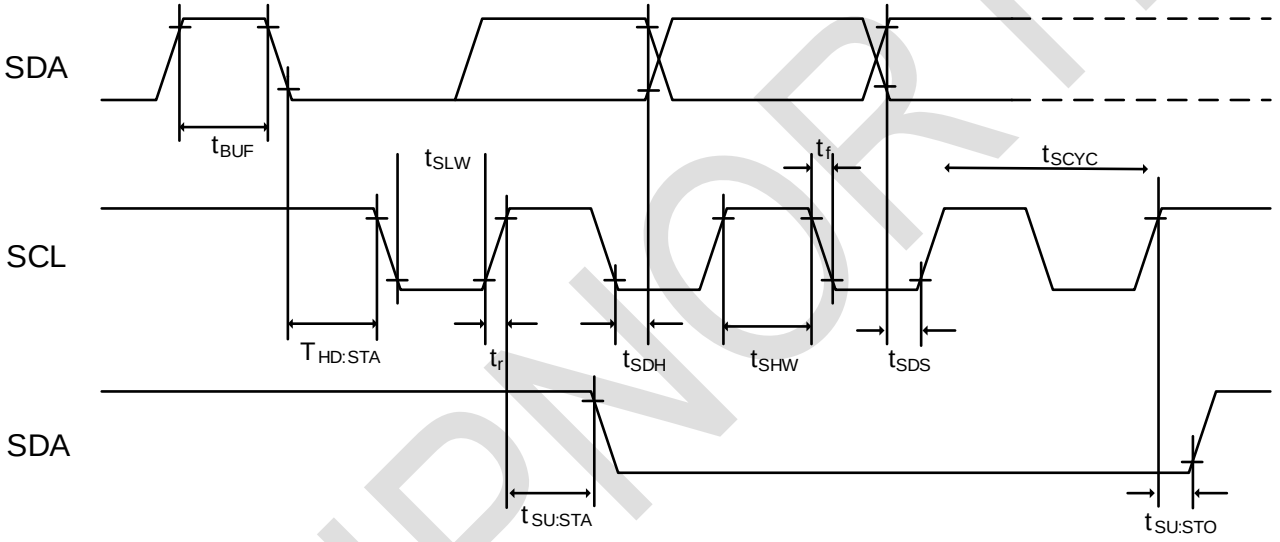
11.2 Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C,unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD Power Range	V_{DD}		2.7	-	5.5	
VLCD Power Range	V_{LCD}	LCD drive voltage, suggest to connect GND	0	-	VDD-2.4	V
"H" Level Input Voltage	V_{IH}		0.7* VDD	-	VDD	V
"L" Level Input Voltage	V_{IL}		VSS	-	0.3*VDD	V
SDA "L" Level Output Voltage	V_{OL_SDA}	I_{LOAD}=-3mA no need to consider the ITO resistance on the COG panel	0	-	0.4	V
COM/SEG ON Resistance	R_{ON}	I_{LOAD}=±10μA	-	3	-	KΩ
Frame Frequency	F_{clk}	FR=65Hz setting	-	80	-	Hz
Standby Current	I_{DD1}	Display off,Oscillation off	-	-	1	uA
Operating Current	I_{DD2}	VDD=3.3V,Ta=25 ℃ ,SR=00,FR=00, Frame inverse,with an LCD panel load.	-	6	20	uA

11.3 MPU Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Rise Time	t_r	-	-	-	0.3	μs
Input Fall Time	t_f	-	-	-	0.3	μs
SCL Cycle Time	t_{SCYC}	-	2.5	-	-	μs
“H” Level SCL Pulse Width	t_{SHW}	-	0.6	-	-	μs
“L” Level SCL Pulse Width	t_{SLW}	-	1.2	-	-	μs
SDA Setup Time	t_{SDS}	-	100	-	-	ns
SDA Hold Time	t_{SDH}	-	100	-	-	ns
Bus Free Time	t_{BUF}	-	1.3	-	-	μs
START Condition Hold Time	$t_{HD;STA}$	-	0.6	-	-	μs
START Condition Setup Time	$t_{SU;STA}$	-	0.6	-	-	μs
STOP Condition Setup Time	$t_{SU;STO}$	-	0.6	-	-	μs



2-line serial interface timing

12 Command Registers Description

	D7	D6	D5	D4	D3	D2	D1	D0
ADSET	**C**	**0**	**0**	P[4:0]				
DISCTL	**C**	**0**	**1**	FR[1:0]		LF	SR[1:0]	
MODSET	**C**	**1**	**0**	ULP	EN	/	/	/
EVRSET	**C**	**1**	**1**	**0**	**0**	EVR[2:0]		
ICSET	**C**	**1**	**1**	**0**	**1**	P[5]	RST	/
BLKCTL	**C**	**1**	**1**	**1**	**0**	BF[2:0]		
APCTL	**C**	**1**	**1**	**1**	**1**	EVR[3]	AON	AOF

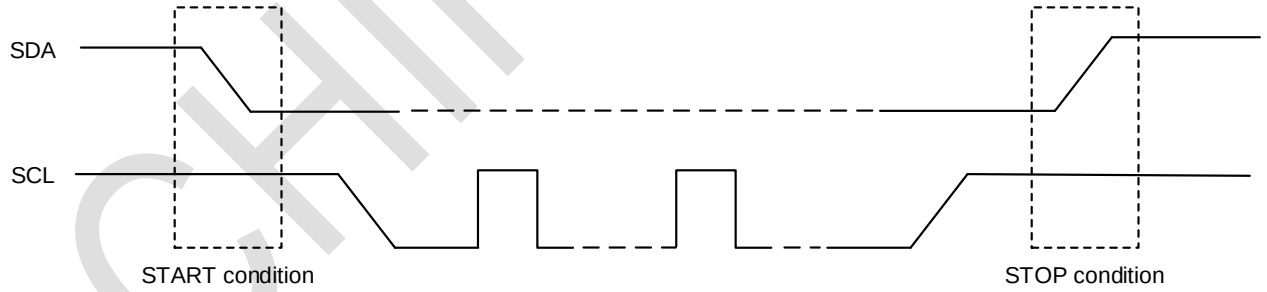
Name	Default	Description
P[5:0]	000000	DDRAM Address. In the write mode, the range of address P [5:0] can be set as 0~2B(Hex). In the read mode, the range of address P [5:0] can be set as 0~2E(Hex). Addresses beyond this range are not allowed, and will be set to "000000". Note: Bit P[5] is in the "ICSET" command.
FR[1:0]	00	Set frame rate according to your needs. 00, 65Hz, Normal Mode 01, 90Hz, Operating Mode1 10, 45Hz, Operating Mode2 11, 130Hz, Operating Mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value. 11, *1.8, High Power Mode
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	Disabling all blocks on the chip; all COM/SEG pins will be pulled to GND. 0: Disabled. 1: Enabled.
EVR[3:0]	0000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * (VDD-VLCD) 0001, 0.975 * (VDD-VLCD) 0010, 0.950 * (VDD-VLCD) 0011, 0.925 * (VDD-VLCD) 0100, 0.900 * (VDD-VLCD) 0101, 0.875 * (VDD-VLCD) 0110, 0.850 * (VDD-VLCD) 0111, 0.825 * (VDD-VLCD) 1000, 0.800 * (VDD-VLCD)

		1001, 0.775 * (VDD-VLCD) 1010, 0.750 * (VDD-VLCD) 1011, 0.725 * (VDD-VLCD) 1100, 0.700 * (VDD-VLCD) 1101, 0.675 * (VDD-VLCD) 1110, 0.650 * (VDD-VLCD) 1111, 0.625 * (VDD-VLCD) Note: The bit EVR[3] is in the command 'APCTL'.
RST	0	Setting '1' resets all command registers in this table but does not reset display data in DDRAM.
BLK[2:0]	000	Config the blink frequency: 000, No blink. 011, 2Hz 001, 0.3Hz 100~111, 1Hz 010, 0.25Hz
AON: AOFF	00	Controlling pixel display: 00, Normal mode. 01, All pixels OFF. Turn off all pixels (independent of DDRAM data). 10, All pixels ON. Turn on all pixels (independent of DDRAM data). 11, Same as '01'. Turn off all pixels (independent of DDRAM data). The AON/AOF command is only effective when the display is enabled (EN=1) and will not alter the DDRAM data.

13 Function Description

13.1 Command and Data Transfer Method

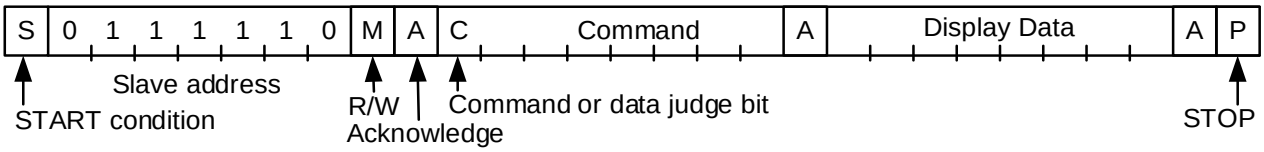
When transmitting commands or data through the 2-wire serial interface, this device must generate "START condition" and "STOP condition" states. When SCL is held high and SDA transitions from a high to a low level, it is considered a "START condition". When SCL is held high and SDA transitions from a low to a high level, it is considered a "STOP condition".



Start and Stop Conditions Diagram

Method of how to transfer command and data is shown as follows.

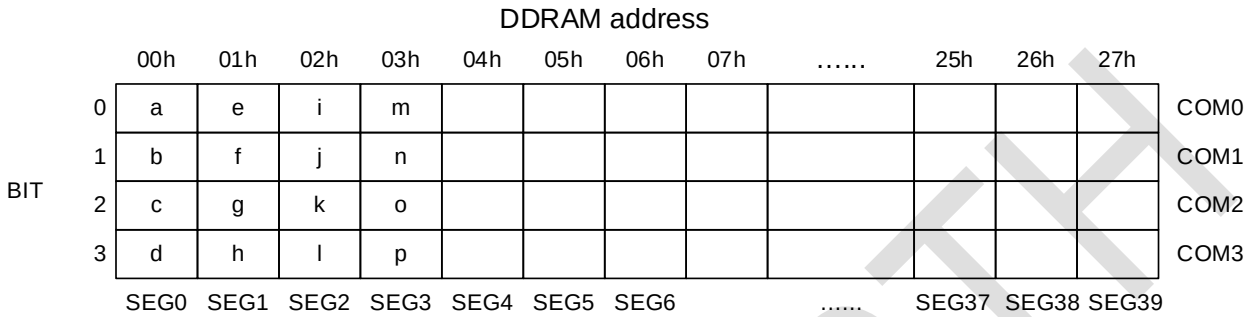
1. Generate "START condition".
2. Issue Slave address 7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"



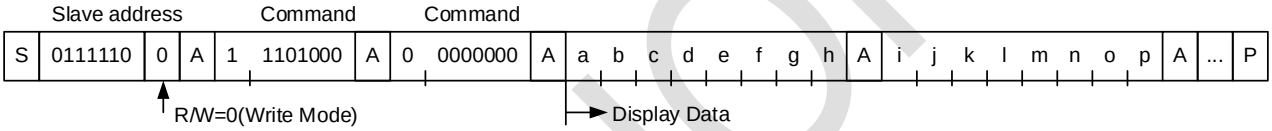
13.2 Write Display Data and Transfer Method

Set R/W bit to '0' to come into write mode.

This device has Display Data RAM (DDRAM) of 40×4=160 bit.

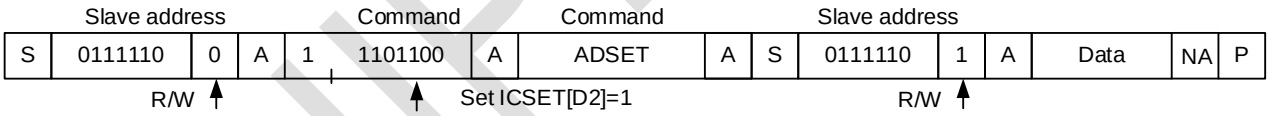


8 bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data. Data can be continuously written in DDRAM by transmitting Data continuously.



13.3 Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data reading sequence.

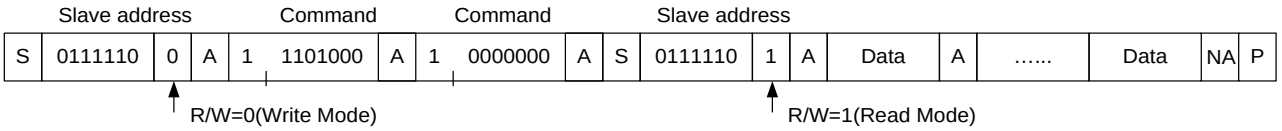


The command register addresses are described below. The following register settings can be read in this mode.

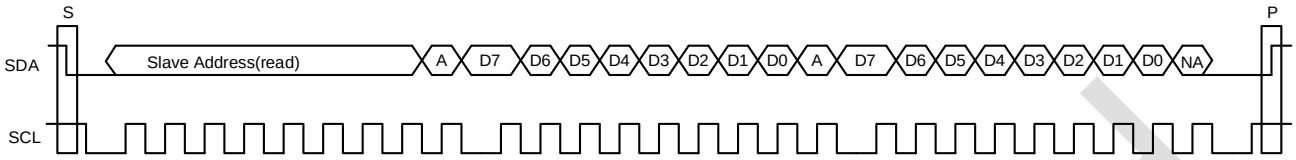
Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BLK[2:0]			2Ch
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOFF	2Dh
REG3	/	/	/	ULP	EVR[3:0]				2Eh

13.4 Read Display Data and Transfer Method

The read mode sequence is shown below.

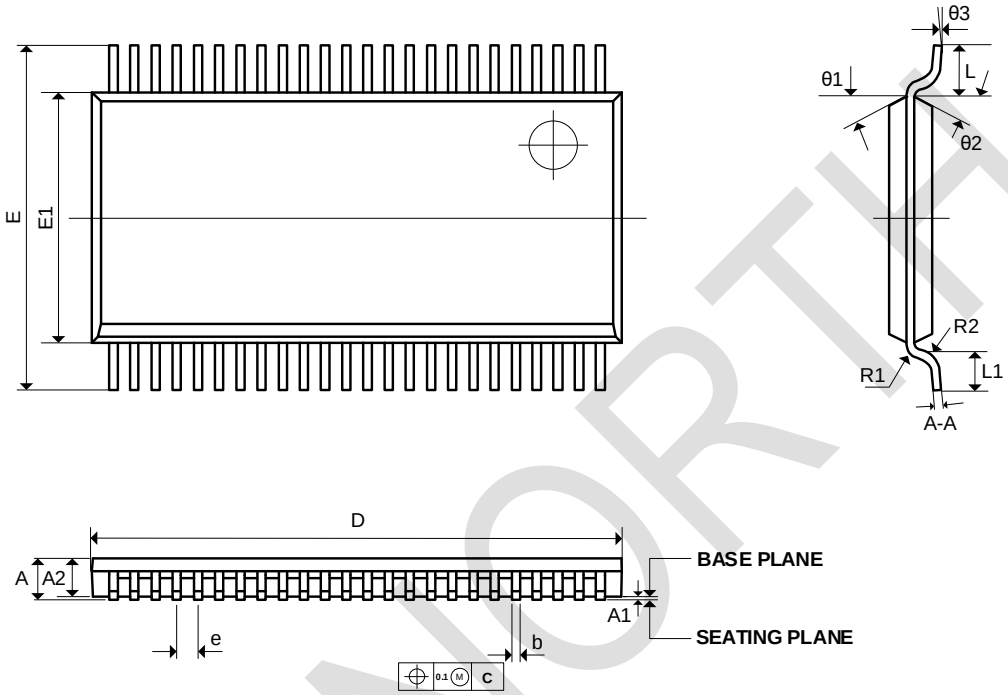


An example of the display data read sequence is shown below.



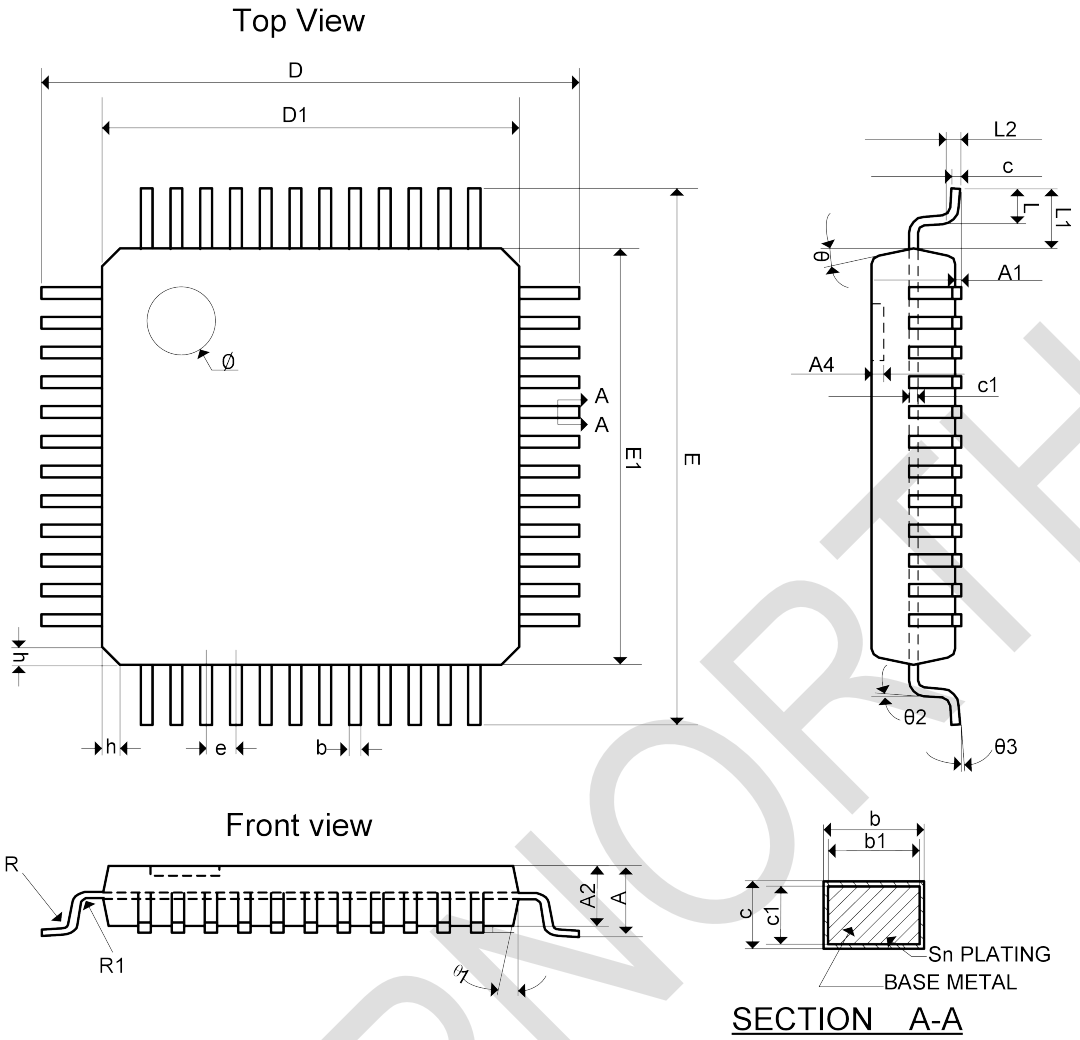
14 Package Information

TSSOP48



SIZE / SYMBOL	MIN (mm)	MAX (mm)	SIZE / SYMBOL	MIN (mm)	MAX (mm)
A		1.2	e	0.5	
A1	0.03	0.13	b	0.17	0.27
A2	0.824	1.024	R1	0.22TYP	
E	7.9	8.3	R2	0.22TYP	
E1	6	6.2	A-A	0.12	0.22
D	12.4	12.6	θ1	12°TYP	
L		1	θ2	12°TYP	
L1	0.35	0.65	θ3	0°	8°

LQFP48



	SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)		SIZE / SYM	MIN (mm)	NOM (mm)	MAX (mm)
TOTAL THICKNESS	A	-	-	1.60	LEAD PITCH	e	0.50BSC		
STAND OFF	A1	0.05	0.10	0.20	CHAMFER	h	0.20	0.30	0.40
BODY THICKNESS	A2	1.35	1.40	1.45	FOOT LENGTH	L	0.45	0.65	0.75
UP BODY THICKNESS	A3	0.64BSC			LEAD LENGTH	L1	1.00BSC		
THIMBLE DEPTH	A4	0.10	0.20	0.30	MEASURE POINT	L2	0.25BSC		
LEAD WIDTH	b	0.17	0.225	0.28	R RADIUS	R	0.15 REF		
LEAD WIDTH	b1	0.20BSC			R1 RADIUS	R1	0.12 REF		
L/F THICKNESS	c	0.127	-	0.16	ANGLE FOR MOLD	θ	12°TYP		
L/F THICKNESS	c1	0.107	0.127	0.147	ANGLE FOR MOLD	θ1	12°TYP		
TOTAL SIZE X	D	8.80	9.00	9.20	ANGLE FOR LEAD	θ2	4°TYP		
BODY SIZE X	D1	6.90	7.00	7.10	ANGLE FOR FOOT	θ3	0°~8°		
TOTAL SIZE Y	E	8.80	9.00	9.20	THIMBLE DIAMETER	Ø	1.10	1.20	1.30
BODY SIZE Y	E1	6.90	7.00	7.10					

15 Important Statement

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