1 Description

The CN9001C4S36 is a segment-type LCD driver chip with a duty cycle of 1/4, capable of driving up to 144 segments. This device incorporates a low-power design, enabling it to achieve ultra-low power consumption and reduce power loss from the power supply.

2 Features

- Low power consumption design, 6uA current at typical condition
- The display mode options include dynamic 1/2and1/3bias voltages, as well as a 1/4duty cycle mode, supporting a maximum of 144 segments.
- The LCD driver chip is integrated with buffer amplifiers.
- supports both register read and display RAM functions.
- incorporates an internal OSC circuit and features a blinking function.
- Integrated Power-on Reset Circuit
- No external component required
- includes an I2C interface
- Compatible with TTL/CMOS
- High EMC immunity

3 Key Specifications

- Supply Voltage Range (VDD): 2.5V to 5.5V
- Supply Voltage Range (VLCD): 0V to (VDD-2.4)V
- Operating Temperature Range: -40°C to +105°C
- Frame Rate (fclk): 80Hz (Typ))

4 Applications

- Home electrical appliance
- Meter equipment et
- Toys
- PDA
- Clocks

5 Ordering information

Product Number	Package	Quantity/Tape
CN9001C4S36	TSSOP48	3500/Reel

6 Marking

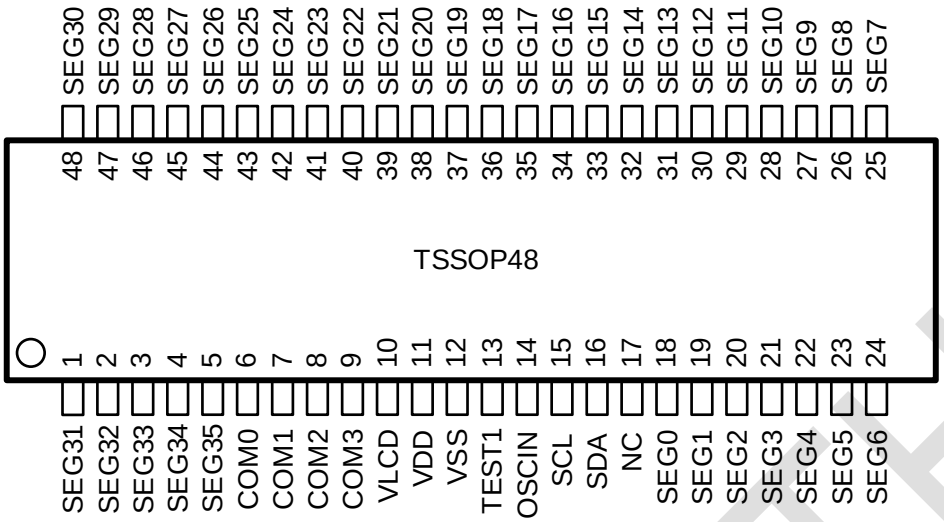
Product Number	Marking
CN9001C4S36	CN9001C4S36 AYYWW

Note: YY=Year WW=Week.

Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

Moisture sensitivity level(MSL):3

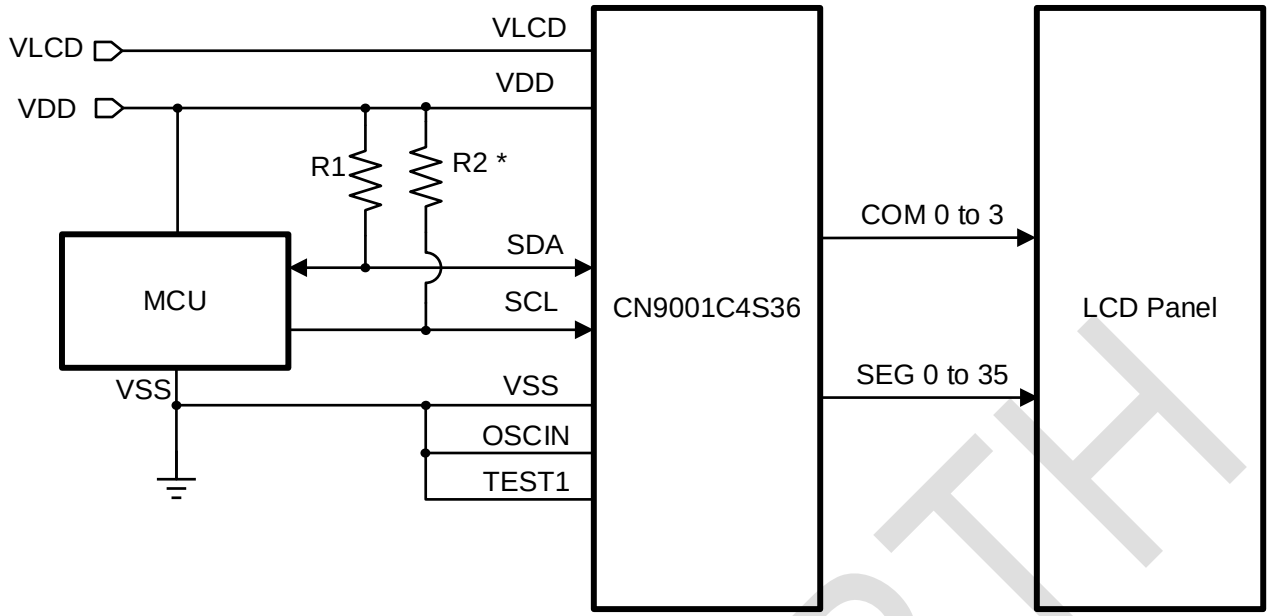
7 Pinout



8 Pin Descriptions

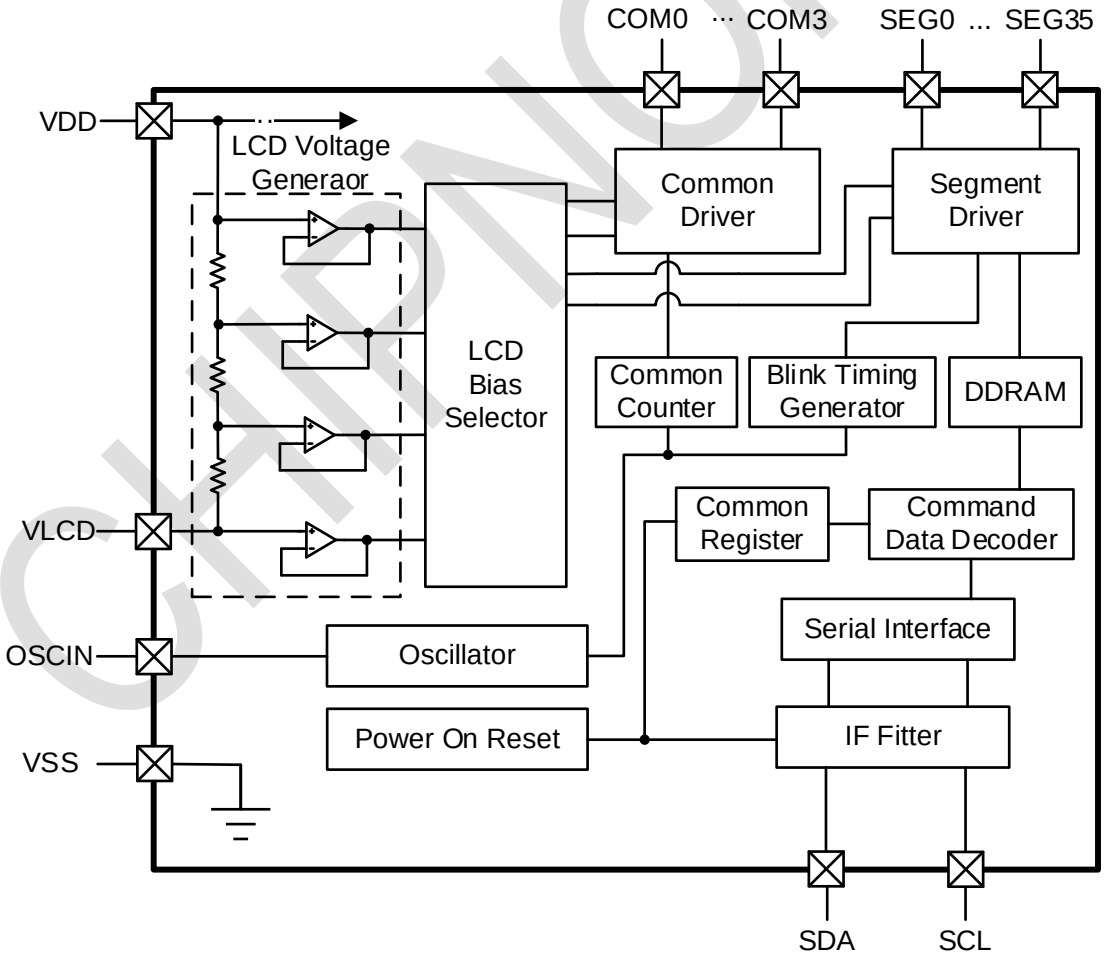
Pin Name	I/O	Pin No.	Descriptions
NC	-	17	Connect to GND
SDA	I/O	16	2-line serial data input and output
SCL	I	15	2-line serial clock input
OSCIN	I	14	External clock input. When using the internal clock, this pin should be grounded.
TEST1	I	13	Test input pin 1, connect to ground.
VSS	I	12	GND
VDD	I	11	Power supply for logic
VLCD	I	10	The default LCD drive voltage is set to a low level
COM 0~3	O	6 ~ 9	COMMON driver output for LCD
SEG 0~35	O	1 ~ 5, 18 ~ 48	SEGMENT driver output for LCD

9 Typical Application



Note: * R2 is optional.

10 Block Diagram



11 Specifications

11.1 Absolute Maximum Ratings

(Vss=0V)

Parameter	Symbol	Rating	Units	Remarks
Power Supply Voltage	V_{DD}	-0.3 to +6.5	V	Power supply
Power Supply Voltage1	V_{LCD}	-0.3 to VDD-2.4	V	LCD drive voltage
Input Voltage Range	V_{IN}	-0.3 to VDD+0.3	V	
Soldering Temperature	T_{lead}	260（soldering,10s）	°C	
Operational Temperature Range	T_{opr}	-40 to +105	°C	
Storage Temperature Range	T_{stg}	-55 to +150	°C	

Note: Operating beyond the absolute maximum rated values may result in IC damage.

11.2 Recommended Operating Conditions

(Ta = +25°C, VSS = 0V, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage	V_{DD}	2.5	-	5.5	V	Power supply
Power Supply Voltage1	V_{LCD}	0	-	VDD-2.4V	V	LCD drive voltage

Note: Please use with VDD-VLCD ≥ 2.5V.

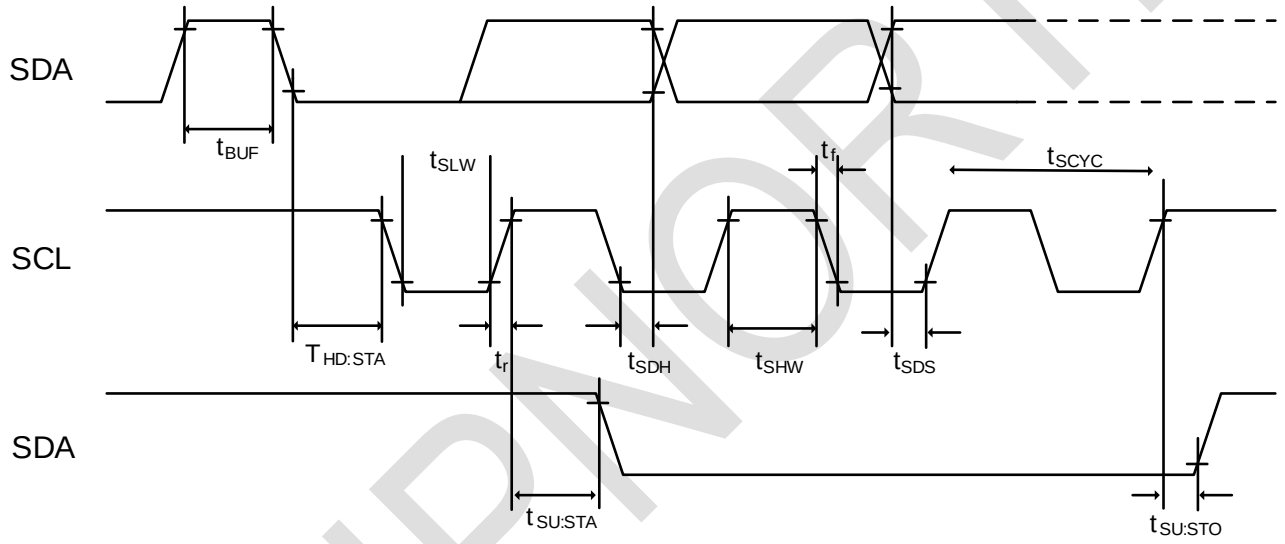
11.3 Electrical Characteristics

DC Characteristics (VDD = 2.5V to 5.5V, VSS = 0V, Ta = -40°C to +105°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
“H” Level Input Voltage	V_{IH}		1.4	-	V_{DD}	V
“L” Level Input Voltage	V_{IL}		V_{SS}	-	0.4	V
“H” Level Input Current	I_{IH}		-	-	1	μA
“L” Level Input Current	I_{IL}		-1	-	-	μA
SDA "L" Level Output Voltage	V_{OL_SDA}	I_{LOAD} = -3mA	0	-	0.4	V
COM/SEG ON Resistance	R_{ON}	I_{LOAD} = ±10μA	-	3	-	kΩ
VLCD Voltage	V_{LCD}	V_{DD}-V_{LCD}≥2.5V	0	-	V_{DD}-2.4	V
Standby Current	I_{DD1}	Display off, Oscillation off	-	-	1	μA
Operating Current	I_{DD2}	VDD=3.3V, Ta=25℃, SR = Power save mode1, FR = Power save mode1, 1/3bias, Frame inversion	-	6	20	μA

11.4 MPU Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Rise Time	t_r	-	-	-	0.3	μs
Input Fall Time	t_f	-	-	-	0.3	μs
SCL Cycle Time	t_{SCYC}	-	2.5	-	-	μs
“H” Level SCL Pulse Width	t_{SHW}	-	0.6	-	-	μs
“L” Level SCL Pulse Width	t_{SLW}	-	1.2	-	-	μs
SDA Setup Time	t_{SDS}	-	100	-	-	ns
SDA Hold Time	t_{SDH}	-	100	-	-	ns
Bus Free Time	t_{BUF}	-	1.3	-	-	μs
START Condition Hold Time	$t_{HD;STA}$	-	0.6	-	-	μs
START Condition Setup Time	$t_{SU;STA}$	-	0.6	-	-	μs
STOP Condition Setup Time	$t_{SU;STO}$	-	0.6	-	-	μs



2-line serial interface timing

11.5 Oscillation Characteristics

(VDD = 2.5V to 5.5V, VSS = 0V, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Frame Frequency	f_{CLK}	56	80	104	Hz	FR= Normal mode

12 Command Registers Description

	D7	D6	D5	D4	D3	D2	D1	D0
ADSET	**C**	**0**	**0**	P[4:0]				
DISCTL	**C**	**0**	**1**	FR[1:0]		LF	SR[1:0]	
MODSET	**C**	**1**	**0**	/	EN	DR	/	/
ICSET	**C**	**1**	**1**	**0**	**1**	P[5]	RST	OC
BLKCTL	**C**	**1**	**1**	**1**	**0**	BLK[2:0]		
APCTL	**C**	**1**	**1**	**1**	**1**	**1**	AON	AOFF

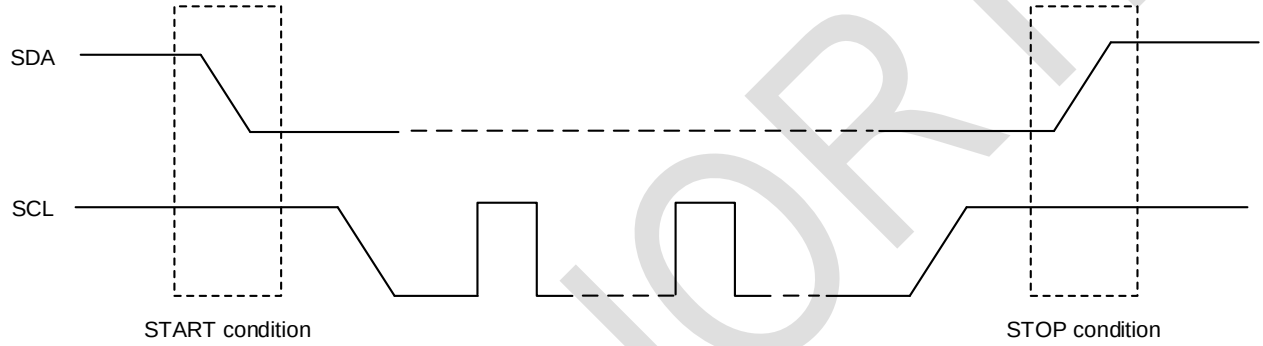
Name	Default	Description
P[5:0]	000000	DDRAM address. The address can be set in the range of 00 to 23 (Hex). Addresses beyond this range are not allowed, and will be set to "000000". Note: Bit P[5] is in the "ICSET" command.
FR[1:0]	00	To conserve power, you can adjust the frame rate.: 00，80Hz，Normal mode 01，70Hz，Power save mode1 10，60Hz，Power save mode2 11，50Hz，Power save mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value. 11, *1.8, High Power Mode
DR	0	Setting Bias Mode: 0, Select 1/3 Bias. 1, Select 1/2 Bias.
EN	0	Disabling all blocks on the chip; all COM/SEG pins will be pulled to GND. 0: Disabled. 1: Enabled.
RST	0	Setting '1' resets all command registers in this table but does not reset display data in DDRAM. Note: Do not simultaneously set P[5] and OC during reset.
OC	0	Setting OSC Mode: 0, Select internal clock. (Connect OSCIN pin to VSS) 1, Select external clock source. (Connect OSCIN pin to external clock source)
BLK[2:0]	000	Config the blink frequency: 000，No blink. 100，0.3Hz. 001，0.5Hz. 101，0.2Hz. 010，1.0Hz. 110，No blink. 011，2.0Hz. 111，No blink.

AON AOF	00	Controlling pixel display: 00, Normal mode. 01, All pixels OFF. Turn off all pixels (independent of DDRAM data). 10, All pixels ON. Turn on all pixels (independent of DDRAM data). 11, Same as '01'. Turn off all pixels (independent of DDRAM data). The AON/AOF command is only effective when the display is enabled (EN=1) and will not alter the DDRAM data.

13 Function Description

13.1 Command and Data Transfer Method

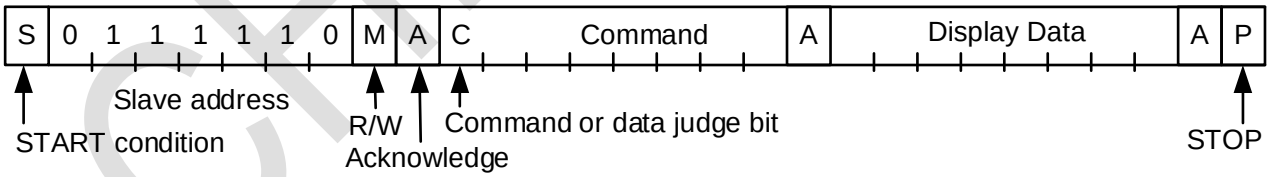
When transmitting commands or data through the 2-wire serial interface, this device must generate "start condition" and "stop condition" states. When SCL is held high and SDA transitions from a high to a low level, it is considered a "start condition" .When SCL is held high and SDA transitions from a low to a high level, it is considered a "stop condition".



Start and Stop Conditions Diagram

Method of how to transfer command and data is shown as follows.

1. Generate “START condition”.
2. Issue Slave address 0x7C.
3. Transfer command.
4. Transfer display data.
5. Generate “STOP condition”.



13.1.1 Acknowledge

When transfer data, always need Acknowledge.

Data format is 8bits and return Acknowledge after transfer 8bits data.

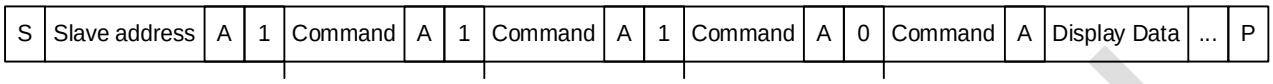
When SCL 8th= "L" after transfer 8bit data (Slave Address, Command, Display Data), output "L"and open SDA line.

When SCL 9th= "L", stop output function. (As Output format is NMOS-Open-Drain, can’t output "H" level.)

If no need Acknowledge function, please input "L" level from SCL 8th= "L" to SCL 9th= "L".

13.1.2 Command Transfer Method

After generating the "start condition", send the slave address "01111100"(write mode), and then immediately transmit the command. The most significant bit (MSB), known as the "command or data indicator bit", defines whether the following byte is a command or data. When the "command or data indicator bit" is set to "1", the next byte is treated as a command. When the "command or data indicator bit" is set to "0", the next byte is considered display data. Setting this flag is crucial because it instructs the device on how to interpret the subsequent bytes as either commands or data.



Once you enter the display data transmission state, no commands can be input. To re-enter a command, you must generate a "start condition" again. If a "start condition" or "stop condition" is entered during the command transmission process, the command will be canceled. Please input the "slave address" in the first data transmission following the "start condition", and it will then be in command input mode.

When the slave address in the first data transmission cannot be recognized, the chip will not respond, and the next transmission will be invalid. When data transmission is in an invalid state and a "start condition" is sent again, it will return to a valid state.

13.1.3 Write Display Data and Transfer Method

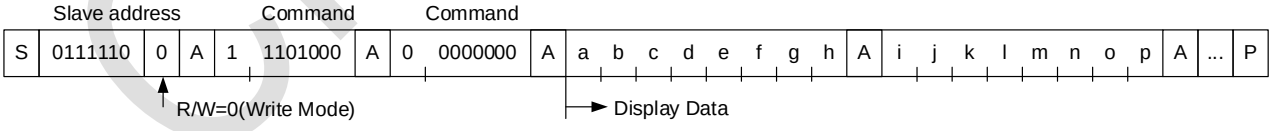
Set R/W bit to "0"to come into write mode.

This device has Display Data RAM (DDRAM) of 36×4=144bit.

DDRAM address

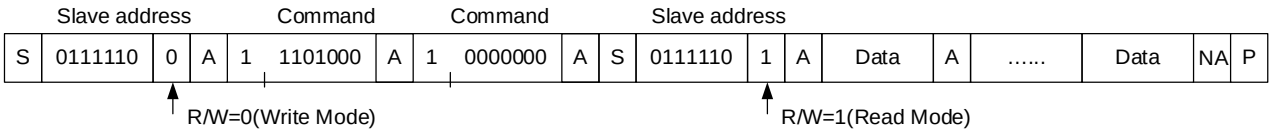
BIT	00	01	02	03	04	05	06	07	…...	21H	22H	23H	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	.....	SEG33	SEG34	SEG35	

8 bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data.



13.1.4 Read Display Data and Transfer Method

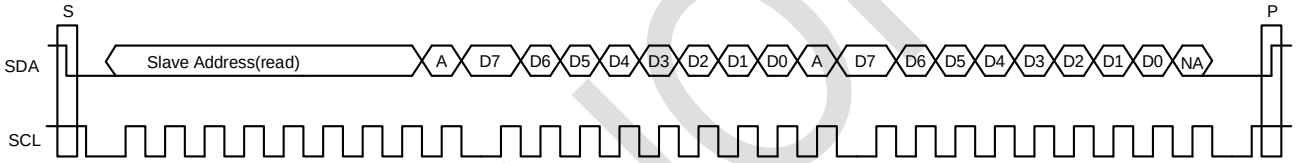
The read mode sequence is shown below.



During read mode, the display data can be read from the DDRAM through the SDA line. The data is outputted serially with SCL input. A write sequence is done first to identify the DDRAM address to be accessed. Then a “START condition” is transmitted again before entering the actual reading of DDRAM data and the Slave Address follows. The display data is outputted continuously afterwards. If no DDRAM address was specified right before the DDRAM read, the output during read mode will be from the current DDRAM address.

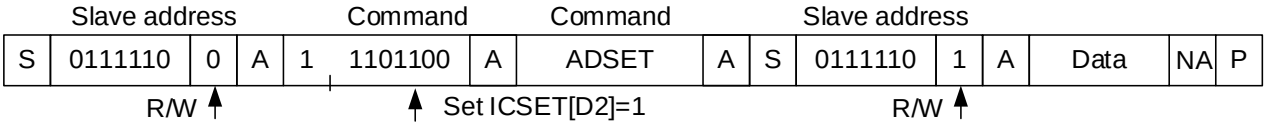
The DDRAM address will increment after every 8-bits of output data. An Acknowledge after every 8-bit of data outputted should be received from the master receiver. This will signal the device that it should continue to output the display data and increment the address. When Non-Acknowledge is received, the device will release the SDA line and the master can then transmit the “STOP condition”. The read mode will be finished once the “STOP condition” is received.

An example of the display data read sequence is shown below.



13.1.5 Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command register read is shown below and is similar to the display data read sequence.



The command register addresses are as follows. In this mode, you can read the following register settings.

Register	D7	D6	D5	D4	D3	D2	D1	D0	address
REG1	0	0	DR	OC	RST	BLK[2:0]			24h
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOFF	25h

13.1.6 Set Address Range

Address map of RAM & register

Write Mode	ADSET				ICSET							
RAM address	D7	D6	D5	P[4:0]	D7	D6	D5	D4	D3	P[5]*	RST	OC
0000 0000 to 0001 1111	0	0	0	0 0000 to 1 1111	1	1	1	0	1	0	0	0
0010 0000 to 0010 0011	0	0	0	0 0000 to 0 0011	1	1	1	0	1	1	0	0

Read Mode	ADSET				ICSET							
RAM address	D7	D6	D5	P[4:0]	D7	D6	D5	D4	D3	P[5]*	RST	OC
0000 0000 to 0001 1111	0	0	0	0 0000 to 1 1111	1	1	1	0	1	0	0	0
0010 0000 to 0010 0101	0	0	0	0 0000 to 0 0101	1	1	1	0	1	1	0	0

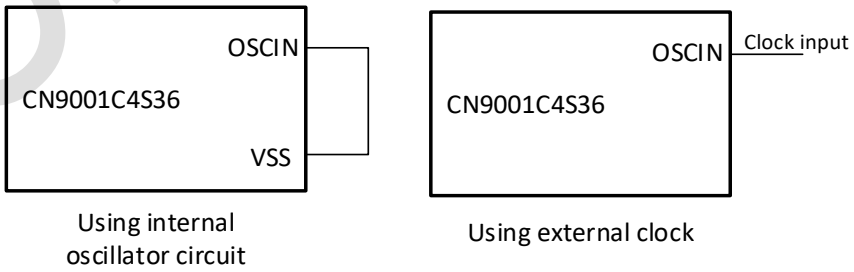
*Note: The setting of the third bit P[5] in ICSET.

13.2 OSCILLATOR

Internal oscillation circuit or an external clock supply can be used as clock source for both logic and analog circuits.

This device has internal oscillator circuit. When you use internal oscillation circuit, please connect OSCIN to VSS.

Note: Please set IC Operation (ICSET) command and connect OSCIN to external clock in using external clock.



13.3 LCD Driver Bias Circuit

This device generates LCD driving voltage by integrated Buffer AMP.

And this device achieves ultra low power consumption.

- 1/3 and 1/2Bias can set in Mode Set (MODSET) command.
- Line and frame inversion mode can be set in Display control (DISCTL) command.

13.4 Blinker Timing Generator

This device has Blinking function.

Blink control (BLKCTL) command put this device into Blink mode.

Blink frequency varies widely by characteristic of f_{CLK} in using internal oscillation circuit.

Refer to “Oscillation Characteristics”for characteristic of f_{CLK}.

13.5 Initialize Sequence

Please follow sequence below after Power-ON to set this device to initial condition.

Power ON

↓

STOP condition

↓

START condition

↓

Issue Slave address

↓

Execute Software Reset by ICSET command

Note that each register value, DDRAM address, and DDRAM data are random after power ON.

13.6 Reset (initial) condition

Initial condition after execute Software Reset is as follows.

（a） Display is OFF. (All SEG & COM status is GND.)

（b） DDRAM address is initialized (DDRAM Data is not initialized)

（c） All registers are restored to their initial default values.

14 Example boot sequence

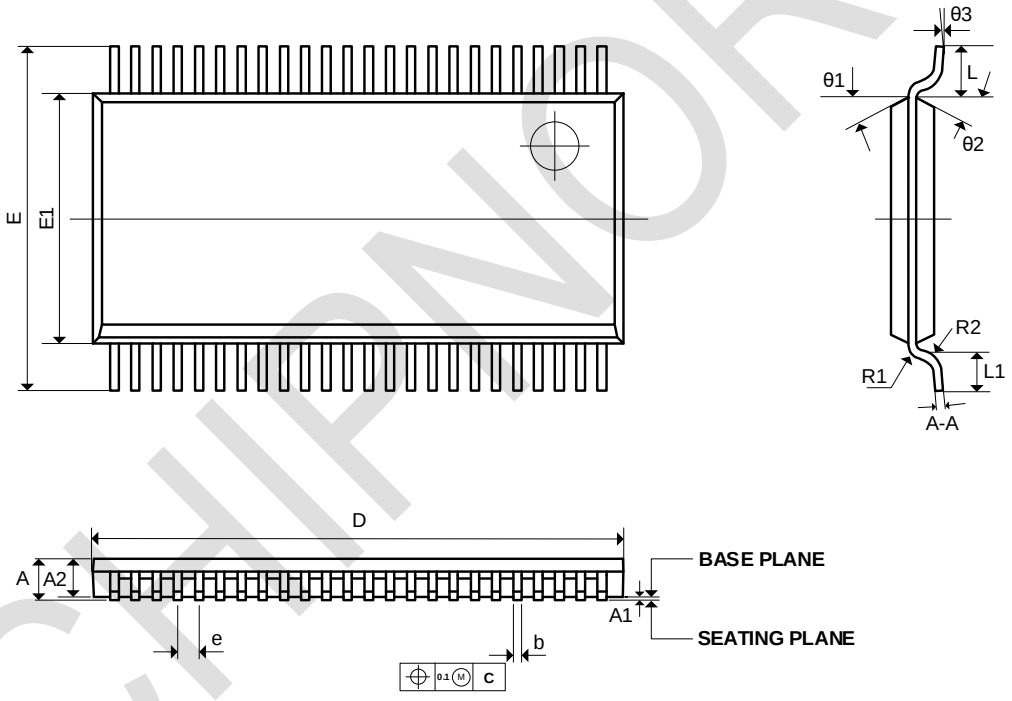
No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power ON									VDD=0 to 5V(tR=0.1ms)
2	wait 100μs									Initialize IC
3	Stop									Stop condition
4	Start									Start condition
5	Slave address	0	1	1	1	1	1	0	0	Issue Slave address
6	ICSET	1	1	1	0	1	0	1	0	Software Reset
7	MODSET	1	1	0	*	1	0	*	*	Display ON
8	DISCTL	1	0	1	0	0	0	1	0	Unnecessary when initial value setup
9	ICSET	1	1	1	0	1	*	0	0	RAM MSB address set
10	ADSET	0	0	0	0	0	0	0	0	RAM address set
11	Display Data	*	*	*	*	*	*	*	*	address 00h-01h
	Display Data	*	*	*	*	*	*	*	*	address 02h-03h
	…									…
	Display Data	*	*	*	*	*	*	*	*	address 22h-23h
12	Stop									Stop condition

15 Package Information

TSSOP48

UNIT:mm

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A		1.2	e	0.5	
A1	0.03	0.13	b	0.17	0.27
A2	0.824	1.024	R1	0.22TYP	
E	7.9	8.3	R2	0.22TYP	
E1	6	6.2	A-A	0.12	0.22
D	12.4	12.6	θ1	12°TYP	
L		1	θ2	12°TYP	
L1	0.35	0.65	θ3	0°	8°



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