

4COM Segment type LCD Driver

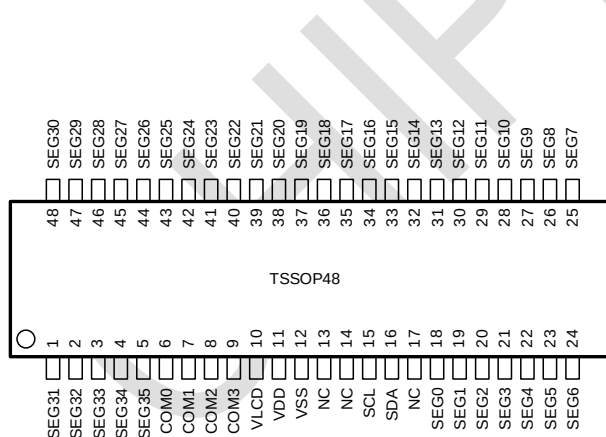
1 Features

- Fixed 1/4 duty mode, 1/3bias voltages supporting a maximum of 160 segments
- Low power consumption design, 6uA current at typical condition
- Incorporates an internal OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Includes an I2C interface
- Compatible with TTL/CMOS
- High EMC immunity

2 Applications

- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

5 Pinout



3 Ordering information

Product Number	Package	Quantity/Tape
CN90C4S40	TSSOP48	2500/Reel

4 Marking

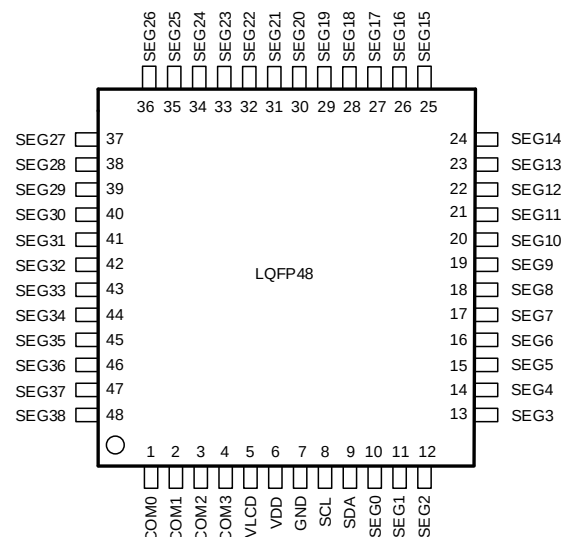
Product Number	Marking
CN90C4S40	CN90C4S40 YYWWAS XXXXXXXX

Note: YY=Year WW=Week AS=Factory code

XXXXXXXX=Wafer lot number

Green (RoHS & HF): CHIPNORTH defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your CHIPNORTH representative directly.

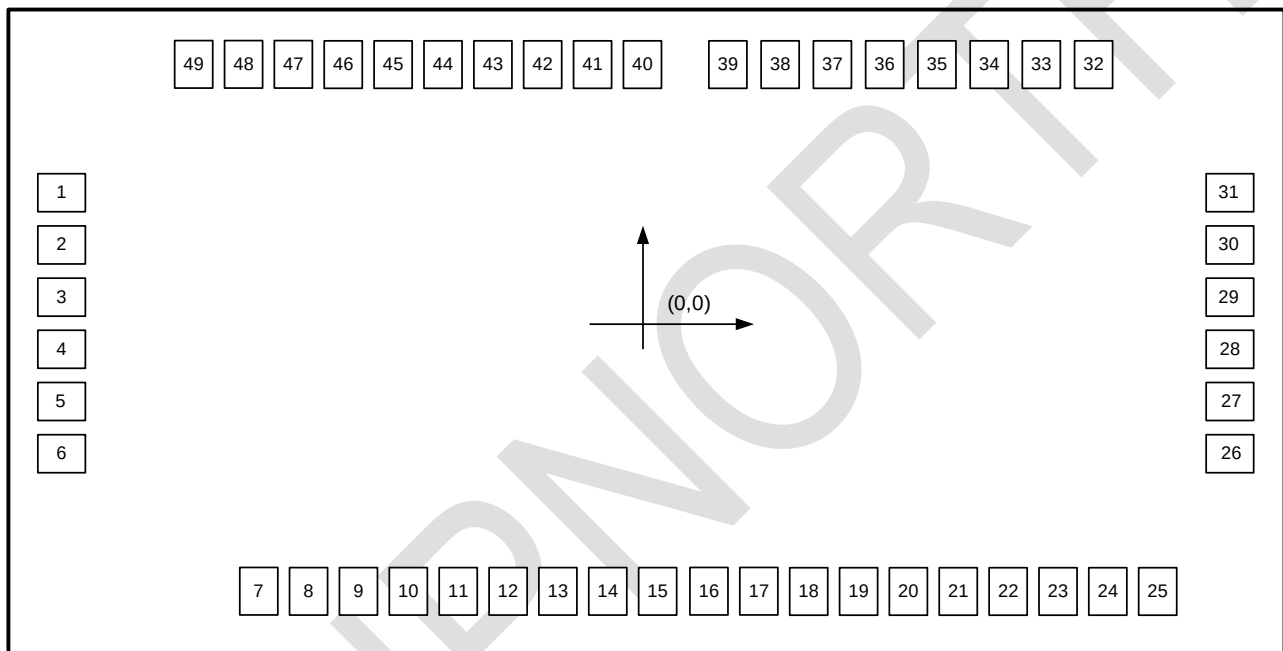
Moisture sensitivity level(MSL):3



6 Pin Descriptions

Pin Name	I/O	TSSOP48	LQFP48	Function
SDA	I/O	16	9	2-line serial data input and output
SCL	I	15	8	2-line serial clock input
VSS	I	12	7	Connect to GND
VDD	I	11	6	Power supply for logic
VLCD	I	10	5	The default LCD drive voltage is set to a low level
SEG0~35	O	18~48,1~5		SEGMENT driver output for LCD
SEG0~38	O		10~48	SEGMENT driver output for LCD
COM0~3	O	6~9	1~4	COMMON driver output for LCD

7 PAD Assignment for COB

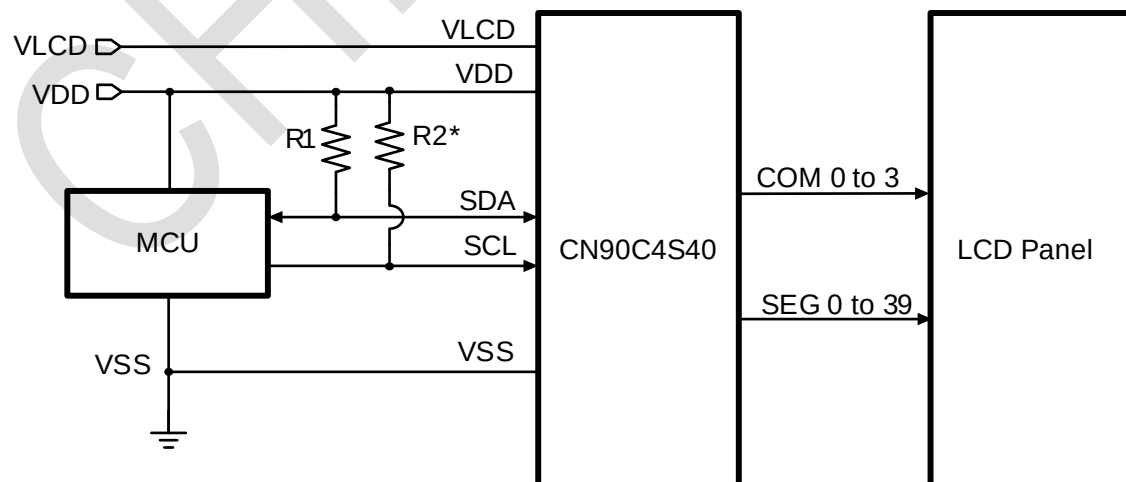


8 PAD Coordinates for COB

UNIT: μm

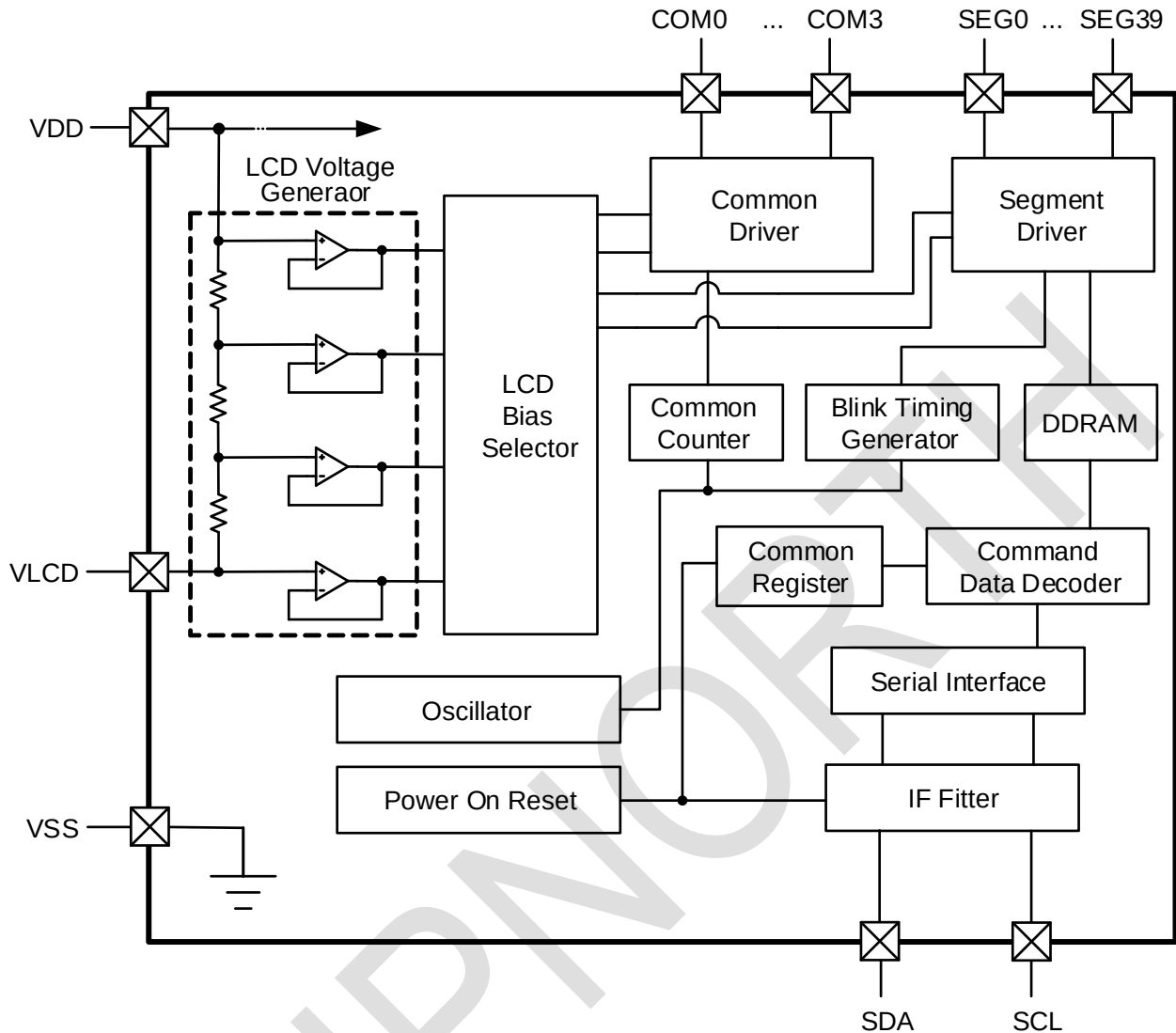
No	Name	X	Y	Size	No	Name	X	Y	Size
1	SEG28	-783	164	60X50	26	SEG4	783	-161	60X50
2	SEG29	-783	99	60X50	27	SEG5	783	-96	60X50
3	SEG30	-783	34	60X50	28	SEG6	783	-31	60X50
4	SEG31	-783	-31	60X50	29	SEG7	783	34	60X50
5	SEG32	-783	-96	60x50	30	SEG8	783	99	60X50
6	SEG33	-783	-161	60X50	31	SEG9	783	164	60X50
7	SEG34	-585	-359	50X60	32	SEG10	584	362	50X60
8	SEG35	-520	-359	50X60	33	SEG11	519	362	50X60
9	SEG36	-455	-359	50X60	34	SEG12	454	362	50X60
10	SEG37	-390	-359	50X60	35	SEG13	389	362	50X60
11	SEG38	-325	-359	50X60	36	SEG14	324	362	50X60
12	SEG39	-260	-359	50X60	37	SEG15	259	362	50X60
13	COM0	-195	-359	50X60	38	SEG16	194	362	50X60
14	COM1	-130	-359	50X60	39	SEG17	129	362	50X60
15	COM2	-65	-359	50X60	40	SEG18	0	362	50X60
16	COM3	0	-359	50X60	41	SEG19	-65	362	50X60
17	VLCD	64	-359	50X60	42	SEG20	-130	362	50X60
18	VDD	129	-359	50X60	43	SEG21	-195	362	50X60
19	GND	194	-359	50X60	44	SEG22	-260	362	50X60
20	SCL	259	-359	50X60	45	SEG23	-325	362	50X60
21	SDA	324	-359	50X60	46	SEG24	-390	362	50X60
22	SEG0	389	-359	50X60	47	SEG25	-455	362	50X60
23	SEG1	454	-359	50X60	48	SEG26	-520	362	50X60
24	SEG2	519	-359	50X60	49	SEG27	-585	362	50X60
25	SEG3	584	-359	50X60					

9 Typical Application



Note: * R2 is optional.

10 Block Diagram



11 Specifications

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Power Supply Voltage	V _{DD}	-0.3 to +6.5	V	Power supply
Power Supply Voltage1	V _{LCD}	-0.3 to V _{DD}	V	LCD drive voltage
Input voltage range	V _{IN}	-0.3 to V _{DD} +0.3	V	
Soldering Temperature	T _{lead}	260 (soldering, 10s)	°C	
Operational temperature range	T _{opr}	-40 to +105	°C	
Storage temperature range	T _{stg}	-55 to +150	°C	

11.2 Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VDD Power Range	V _{DD}		2.7	-	5.5	
VLCD Power Range	V _{LCD}	LCD drive voltage, suggest to connect GND	0	-	VDD-2.4	V
"H" Level Input Voltage	V _{IH}		0.7* VDD	-	VDD	V
"L" Level Input Voltage	V _{IL}		VSS	-	0.3*VDD	V
SDA "L" Level Output Voltage	V _{OL_SDA}	I _{LOAD} =-3mA no need to consider the ITO resistance on the COG panel	0	-	0.4	V
COM/SEG ON Resistance	R _{ON}	I _{LOAD} =±10μA	-	3	-	KΩ
Frame Frequency	F _{clk}	FR=80Hz setting	-	80	-	Hz
Standby Current	I _{DD1}	Display off, Oscillation off	-	-	1	uA
Operating Current	I _{DD2}	VDD=3.3V, Ta=25 °C ,SR=00,FR=00, Frame inverse, with an LCD panel load.	-	6	20	uA

12 Command Registers Description

	D7	D6	D5	D4	D3	D2	D1	D0
ADSET	C	0	0	P[4:0]				
DISCTL	C	0	1	FR[1:0]		LF	SR[1:0]	
MODSET	C	1	0	ULP	EN	/	/	/
EVRSET	C	1	1	0	0	EV[2:0]		
ICSET	C	1	1	0	1	P[5]	RST	/
BLKCTL	C	1	1	1	0	BF[2:0]		
APCTL	C	1	1	1	1	EV[3]	AON	AOF

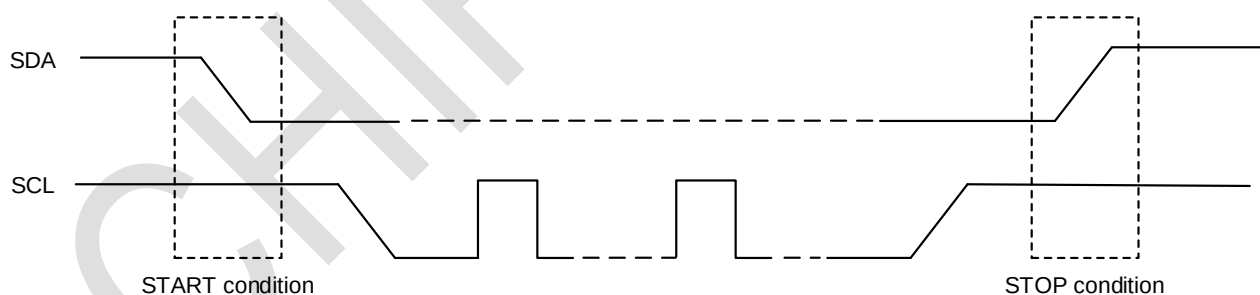
Name	Default	Description
P[5:0]	000000	DDRAM Address. In the write mode, the range of address P [5:0] can be set as 0~2B(Hex). In the read mode, the range of address P [5:0] can be set as 0~2E(Hex). Addresses beyond this range are not allowed, and will be set to "000000". Note: Bit P[5] is in the "ICSET" command.
FR[1:0]	00	Set frame rate according to your needs. 00, 65Hz, Normal Mode 01, 90Hz, Operating Mode1 10, 45Hz, Operating Mode2 11, 130Hz, Operating Mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value. 11, *1.8, High Power Mode
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	Disabling all blocks on the chip; all COM/SEG pins will be pulled to GND. 0: Disabled. 1: Enabled.
EV[3:0]	0000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * (VDD-VLCD) 0001, 0.975 * (VDD-VLCD) 0010, 0.950 * (VDD-VLCD) 0011, 0.925 * (VDD-VLCD) 0100, 0.900 * (VDD-VLCD) 0101, 0.875 * (VDD-VLCD) 0110, 0.850 * (VDD-VLCD) 0111, 0.825 * (VDD-VLCD) 1000, 0.800 * (VDD-VLCD)

		1001, 0.775 * (VDD-VLCD) 1010, 0.750 * (VDD-VLCD) 1011, 0.725 * (VDD-VLCD) 1100, 0.700 * (VDD-VLCD) 1101, 0.675 * (VDD-VLCD) 1110, 0.650 * (VDD-VLCD) 1111, 0.625 * (VDD-VLCD) Note: The bit EV[3] is in the command 'APCTL'.
RST	0	Setting '1' resets all command registers in this table but does not reset display data in DDRAM.
BF[2:0]	000	Config the blink frequency: 000, No blink. 011, 2Hz 001, 0.3Hz 100~111, 1Hz 010, 0.25Hz
AON: AOFF	00	Controlling pixel display: 00, Normal mode. 01, All pixels OFF. Turn off all pixels (independent of DDRAM data). 10, All pixels ON. Turn on all pixels (independent of DDRAM data). 11, Same as '01'. Turn off all pixels (independent of DDRAM data). The AON/AOF command is only effective when the display is enabled (EN=1) and will not alter the DDRAM data.

13 Function Description

13.1 Command and Data Transfer Method

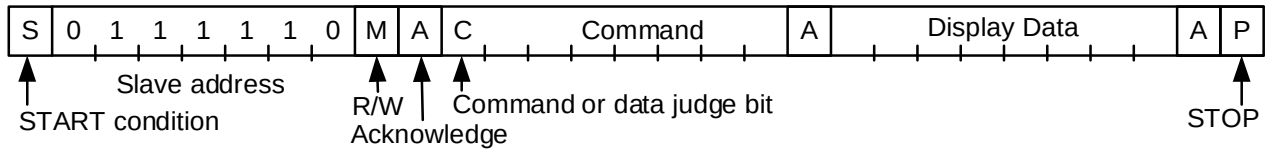
When transmitting commands or data through the 2-wire serial interface, this device must generate "start condition" and "stop condition" states. When SCL is held high and SDA transitions from a high to a low level, it is considered a "start condition". When SCL is held high and SDA transitions from a low to a high level, it is considered a "stop condition".



Start and Stop Conditions Diagram

Method of how to transfer command and data is shown as follows.

1. Generate "START condition".
2. Issue Slave address 7C.
3. Transfer command.
4. Transfer display data.
5. Generate "STOP condition"



13.2 Write Display Data and Transfer Method

Set R/W bit to '0' to come into write mode.

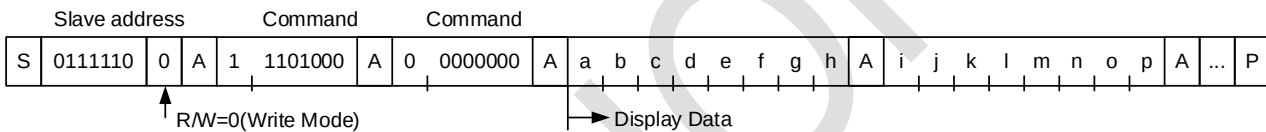
This device has Display Data RAM (DDRAM) of 40×4=160 bit.

DDRAM address												
	00	01	02	03	04	05	06	07		25H	26H	27H
0	a	e	i	m								
1	b	f	j	n								
2	c	g	k	o								
3	d	h	l	p								
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6			SEG37	SEG38	SEG39

BIT

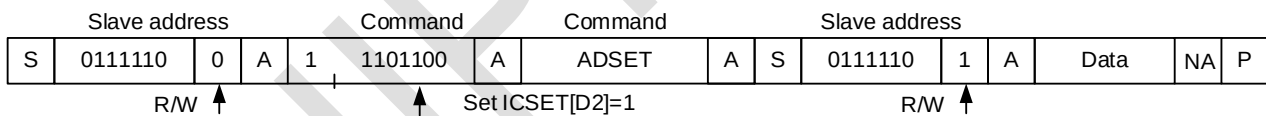
COM0
COM1
COM2
COM3

8 bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data. Data can be continuously written in DDRAM by transmitting Data continuously.



13.3 Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data reading sequence.

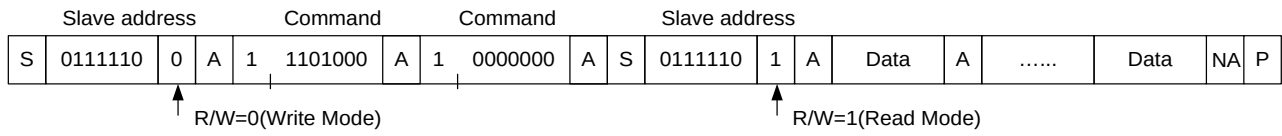


The command register addresses are described below. The following register settings can be read in this mode.

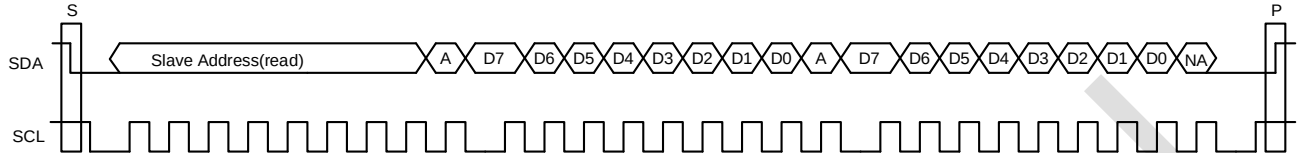
Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			2CH
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOF	2DH
REG3	/	/	/	ULP	EV[3:0]				2EH

13.4 Read Display Data and Transfer Method

The read mode sequence is shown below.

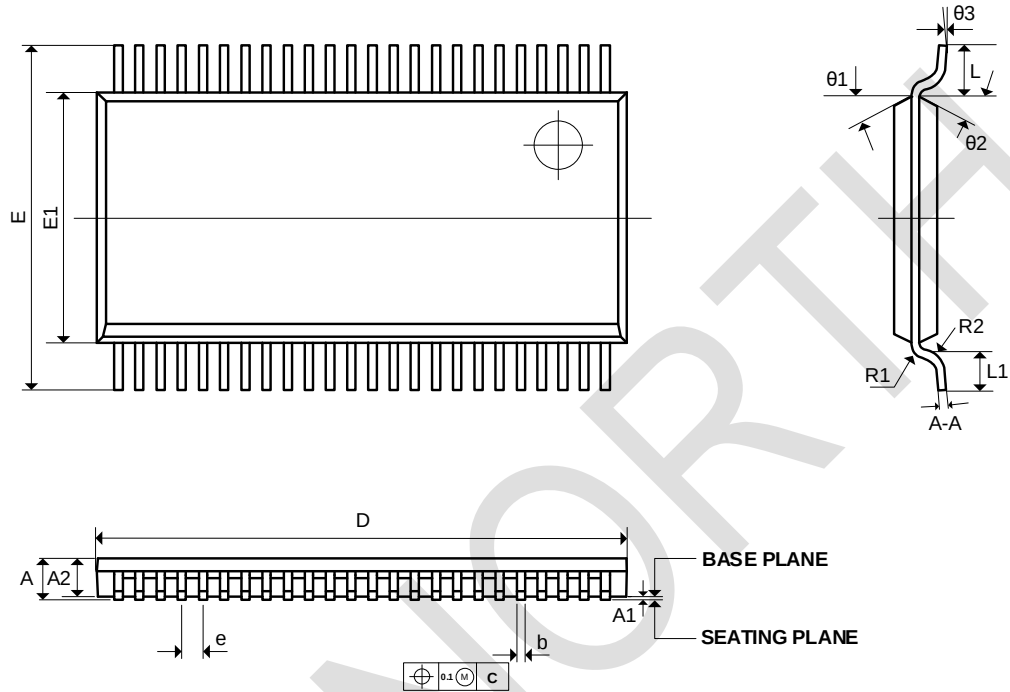


An example of the display data read sequence is shown below.



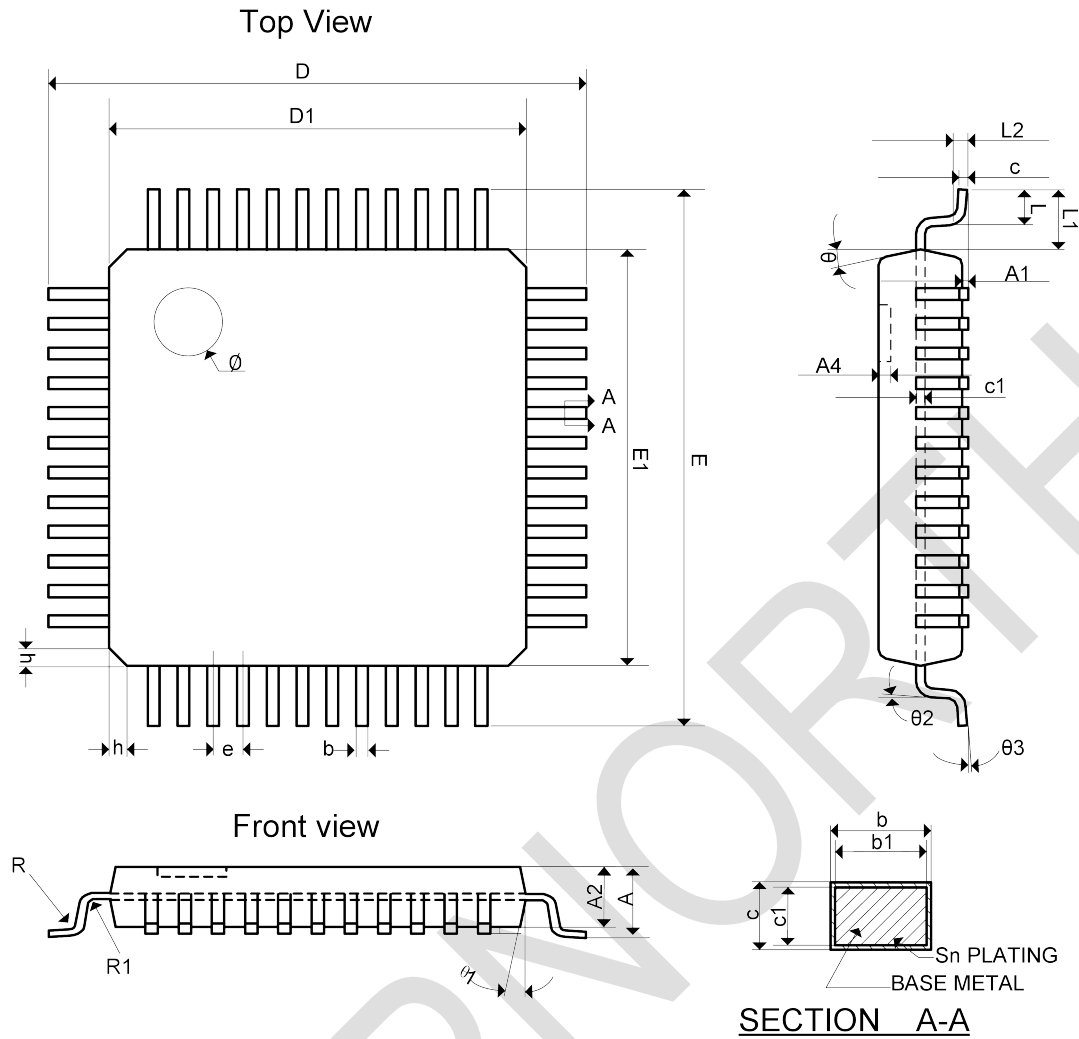
14 Package Information

TSSOP48



SIZE SYMBOL	MIN (mm)	MAX (mm)	SIZE SYMBOL	MIN (mm)	MAX (mm)
A		1.2	e	0.5	
A1	0.03	0.13	b	0.17	0.27
A2	0.824	1.024	R1	0.22TYP	
E	7.9	8.3	R2	0.22TYP	
E1	6	6.2	A-A	0.12	0.22
D	12.4	12.6	θ1	12°TYP	
L		1	θ2	12°TYP	
L1	0.35	0.65	θ3	0°	8°

LQFP48



	SIZE SYM	MIN (mm)	NOM (mm)	MAX (mm)		SIZE SYM	MIN (mm)	NOM (mm)	MAX (mm)
TOTAL THICKNESS	A	-	-	1.60	LEAD PITCH	e	0.50BSC		
STAND OFF	A1	0.05	0.10	0.20	CHAMFER	h	0.20	0.30	0.40
BODY THICKNESS	A2	1.35	1.40	1.45	FOOT LENGTH	L	0.45	0.65	0.75
UP BODY THICKNESS	A3	0.64BSC			LEAD LENGTH	L1	1.00BSC		
THIMBLE DEPTH	A4	0.10	0.20	0.30	MEASURE POINT	L2	0.25BSC		
LEAD WIDTH	b	0.17	0.225	0.28	R RADIUS	R	0.15 REF		
LEAD WIDTH	b1	0.20BSC			R1 RADIUS	R1	0.12 REF		
L/F THICKNESS	c	0.127	-	0.16	ANGLE FOR MOLD	θ	12°TYP		
L/F THICKNESS	c1	0.107	0.127	0.147	ANGLE FOR MOLD	θ1	12°TYP		
TOTAL SIZE X	D	8.80	9.00	9.20	ANGLE FOR LEAD	θ2	4°TYP		
BODY SIZE X	D1	6.90	7.00	7.10	ANGLE FOR FOOT	θ3	0°~8°		
TOTAL SIZE Y	E	8.80	9.00	9.20	THIMBLE DIAMETER	Ø	1.10	1.20	1.30
BODY SIZE Y	E1	6.90	7.00	7.10					

15 Important Statement

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